High Frequency 6.6kW Bi-directional On Board Charger for Plug-in Hybrid Electrical Vehicle

D3.2

Bench 26

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U.S. DEPARTMENT OF ENERGY

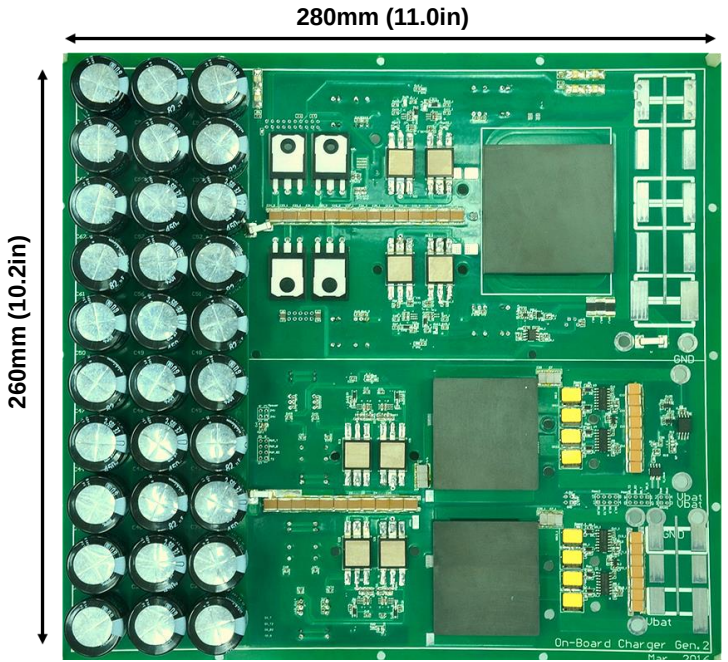
Project funded by DOE Award Number DE-EE0006834, through Delta Products Corp

Prime applicant and project lead

More advanced technology development

GaN device development

In-vehicle evaluation



PFC (>300kHz)

Height: 40mm (1.6in) w/ cold plate

DC/DC(~500kHz)

- **37W/in^3 high power density**
- **>96% Efficiency over whole battery voltage**

State-of-Art On Board Charger and CPES Target

Efficiency

96%

94%

92%

90%

Power Density

0W/in³ 5W/in³ 10W/in³ 15W/in³ 20W/in³ 25W/in³

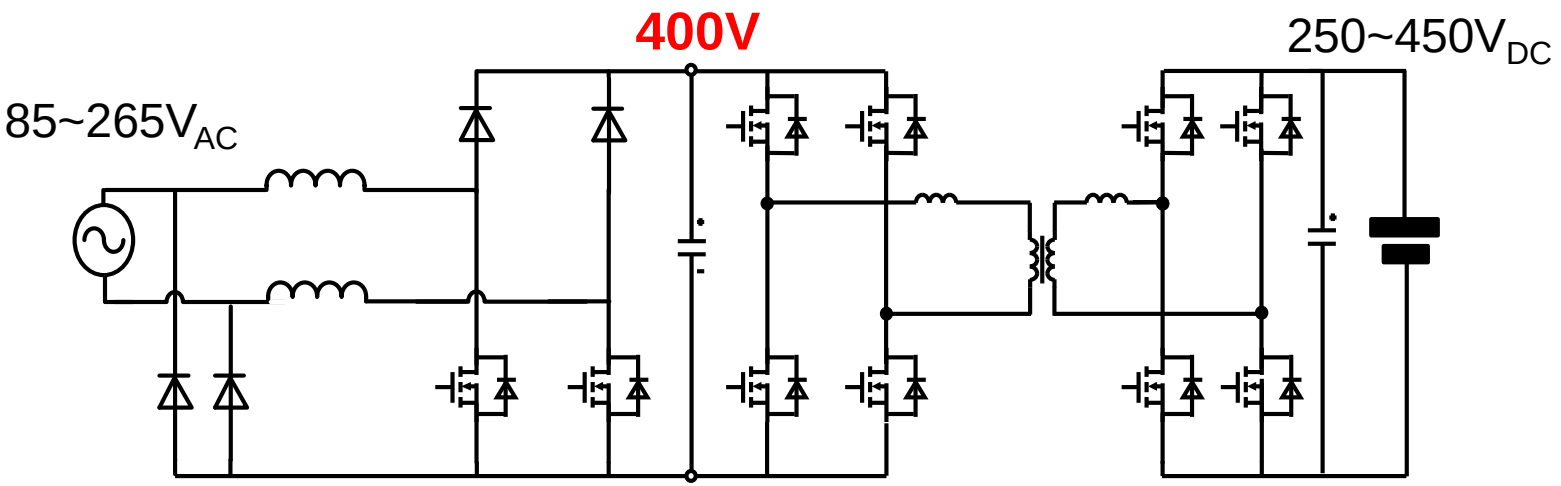
Si Device <100kHz
3~12W/in³
92~94% Efficiency
Uni-directional

CPES

Wide Band Gap Device
>300kHz
>25W/in³
>95% Efficiency
Bi-directional

Conventional Si-Based On Board Charger

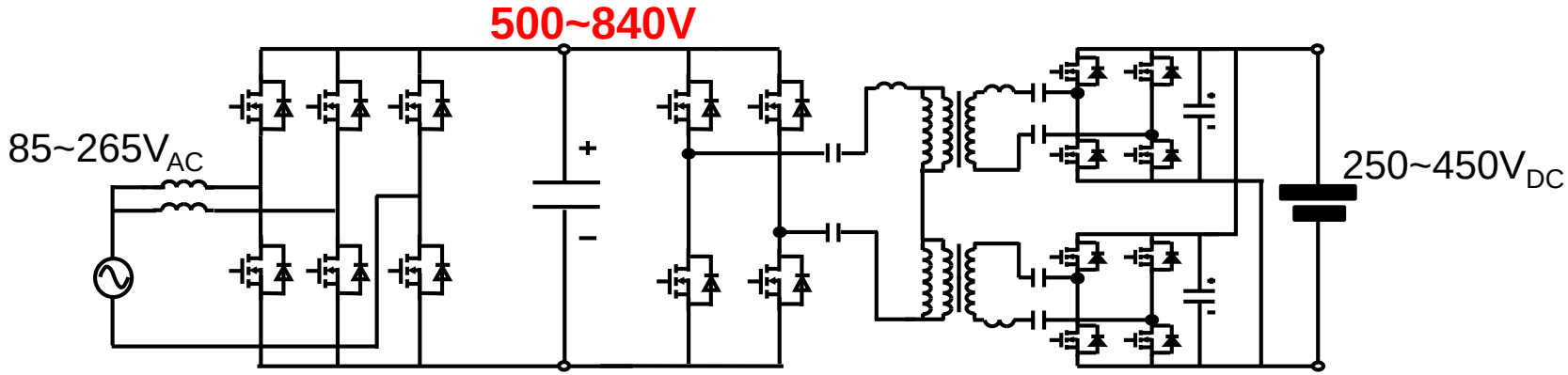
Si based design: Uni-direction



Dual Boost PFC (CCM)
<70kHz 98% peak eff.

Dual Active Bridge (DAB)
200kHz 96% peak eff.

Bi-directional On Board Charger



1.2kV SiC
>300kHz 98%~99% eff.

1.2kV SiC
500kHz 98% eff.

650V GaN
500kHz

- PFC/inverter
- CRM ZVS
- 2 phase interleaving
- Unified control

- Variable DC-Link
- track battery voltage
- shift regulation burden

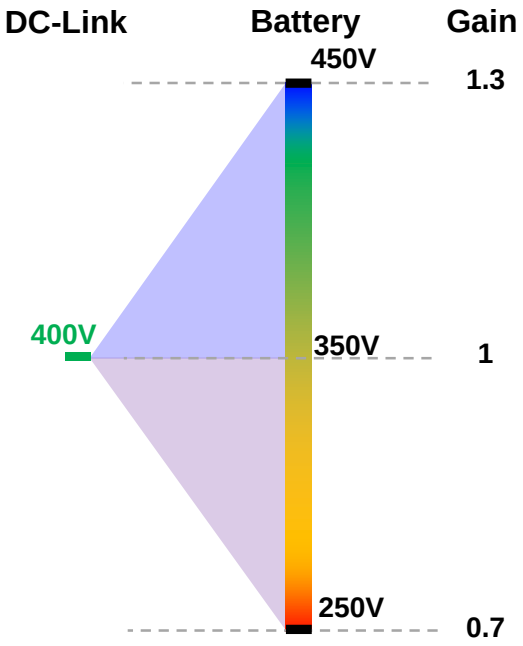
- 6 layer PCB
- Integrated magnetic (4 inductor + 1 transformer)
- CM noise reduction

- Bi-direction CLLC
- ZVS and ZCS

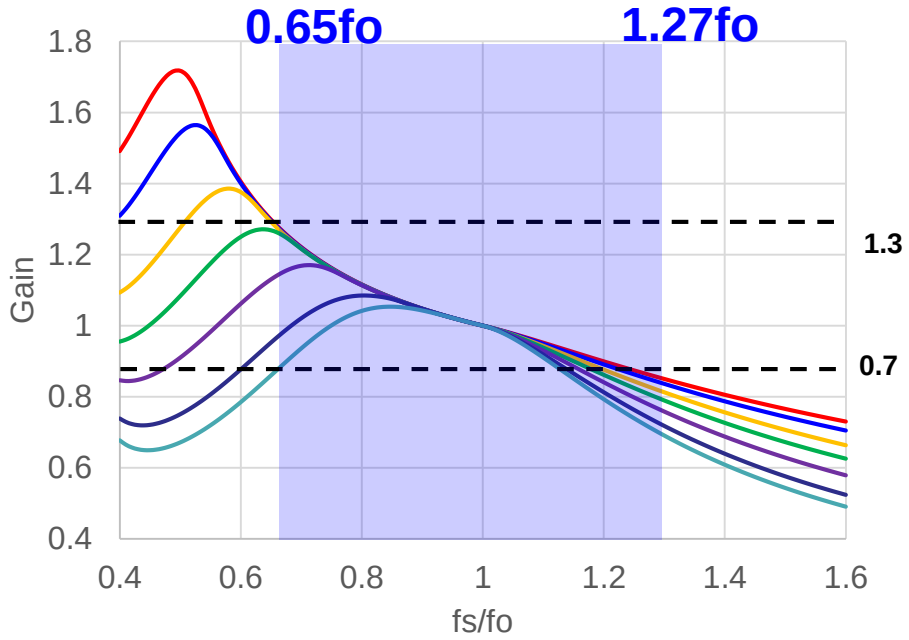
❑>96% all range eff. with 37W/in^3 power density
❑Very good manufacturability using PCB magnetic

Limitation of Base Line Design

Gain Range for CLLC

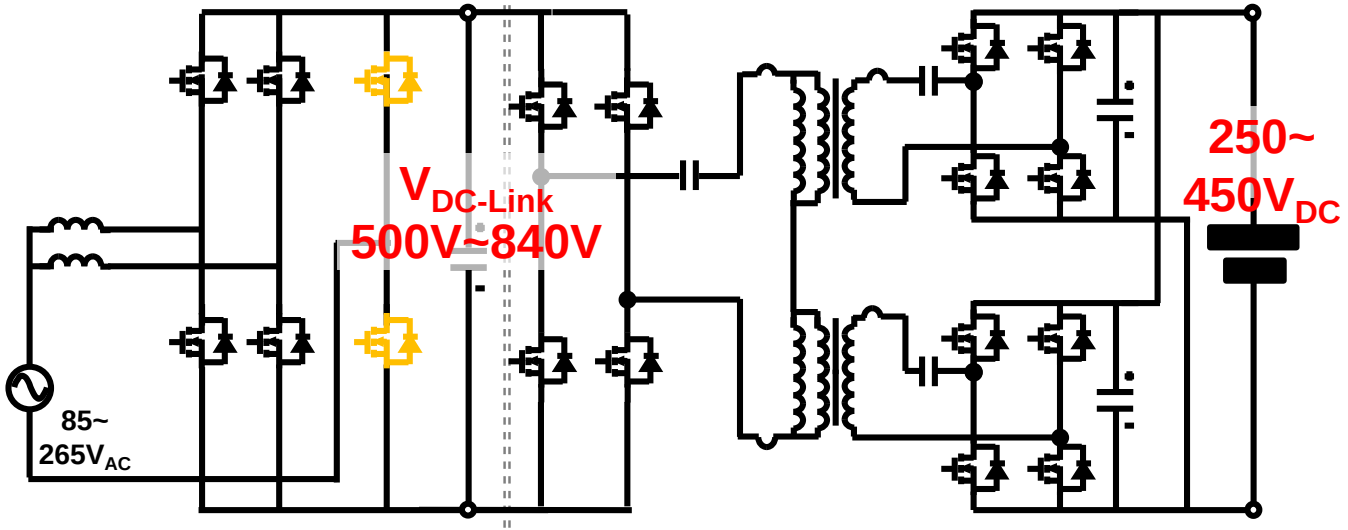


Frequency Range for CLLC



Very wide frequency range of DC/DC stage

CPES Design: Variable DC-Link

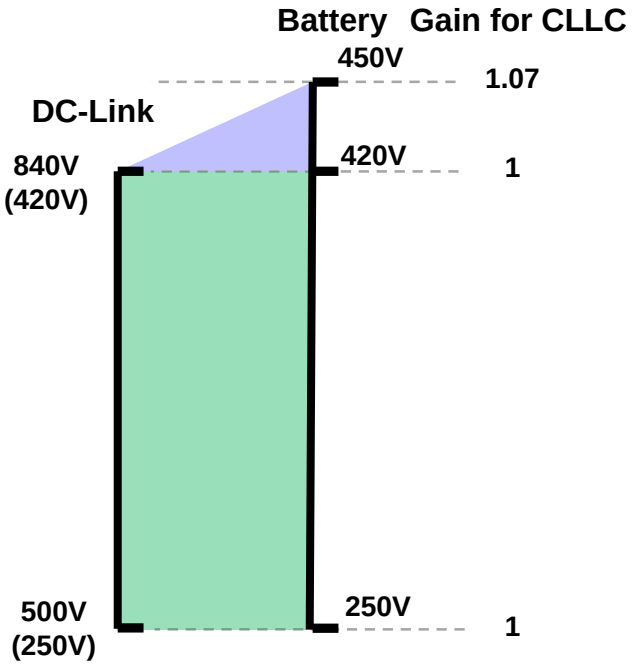


1st Stage: Totem-pole PFC (CRM ZVS operation)

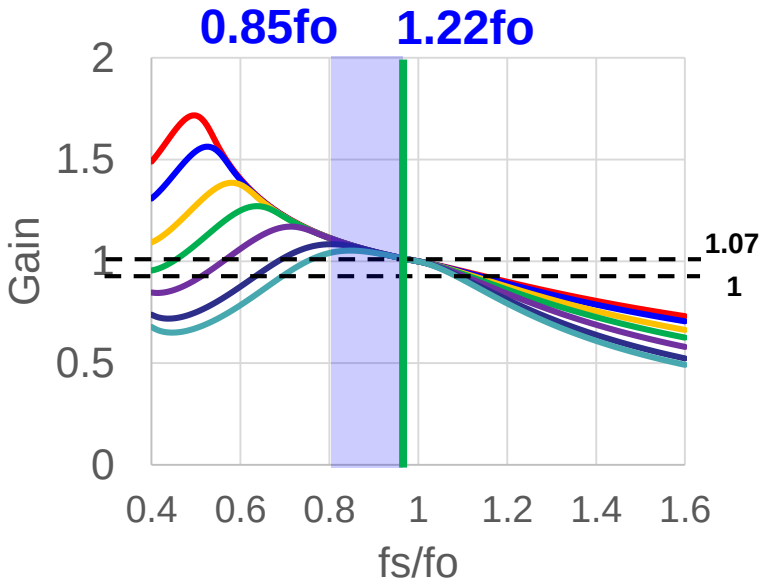
2nd Stage: CLLC (ZVS ZCS Operation)

Gain Range Comparison

Gain Range for CLLC

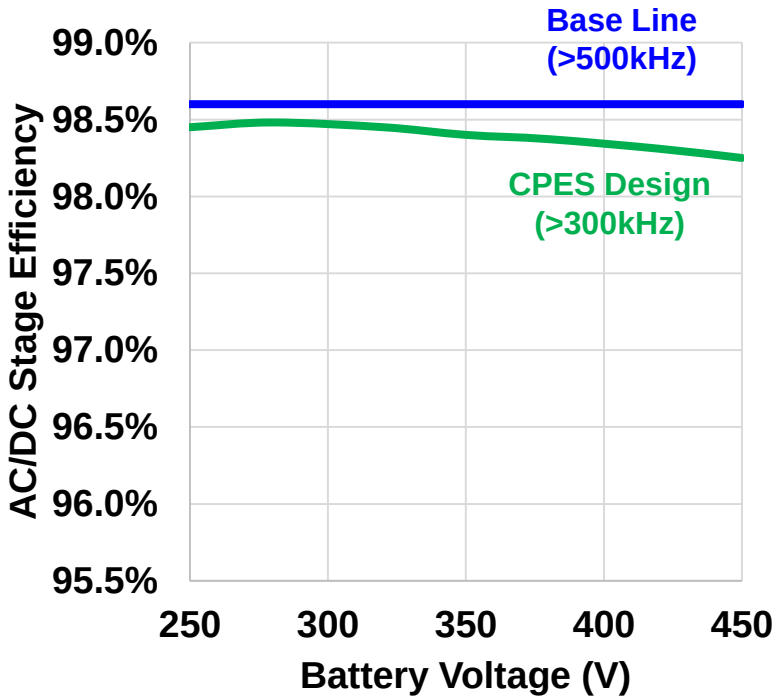


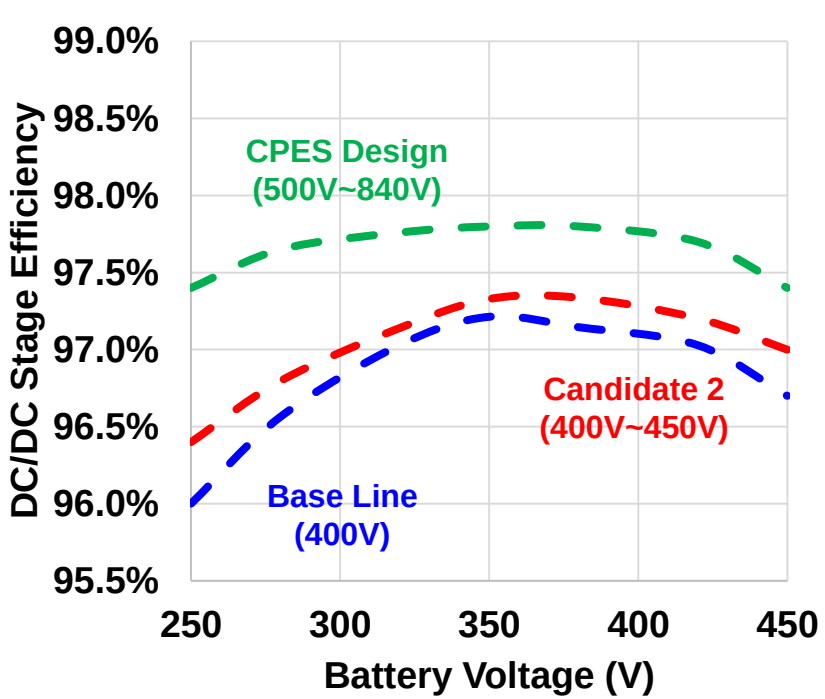
Frequency Range for CLLC



Further Reduced gain range and frequency range

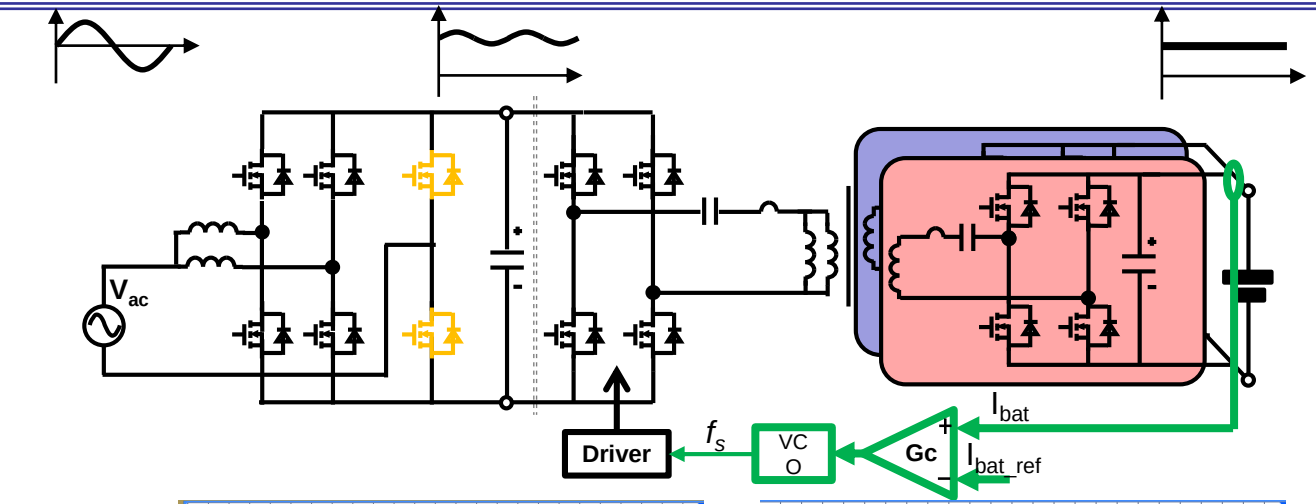
AC/DC and DC/DC Efficiency Evaluation

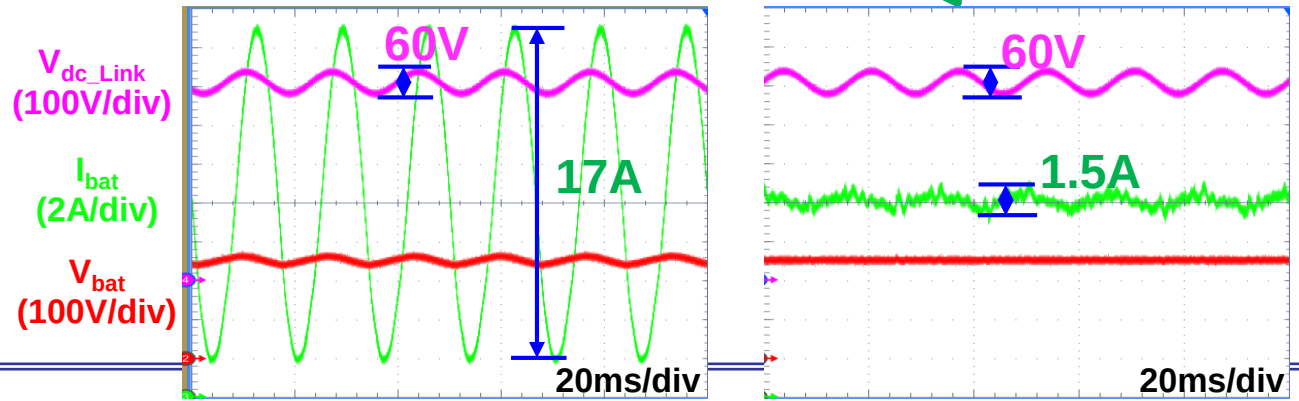




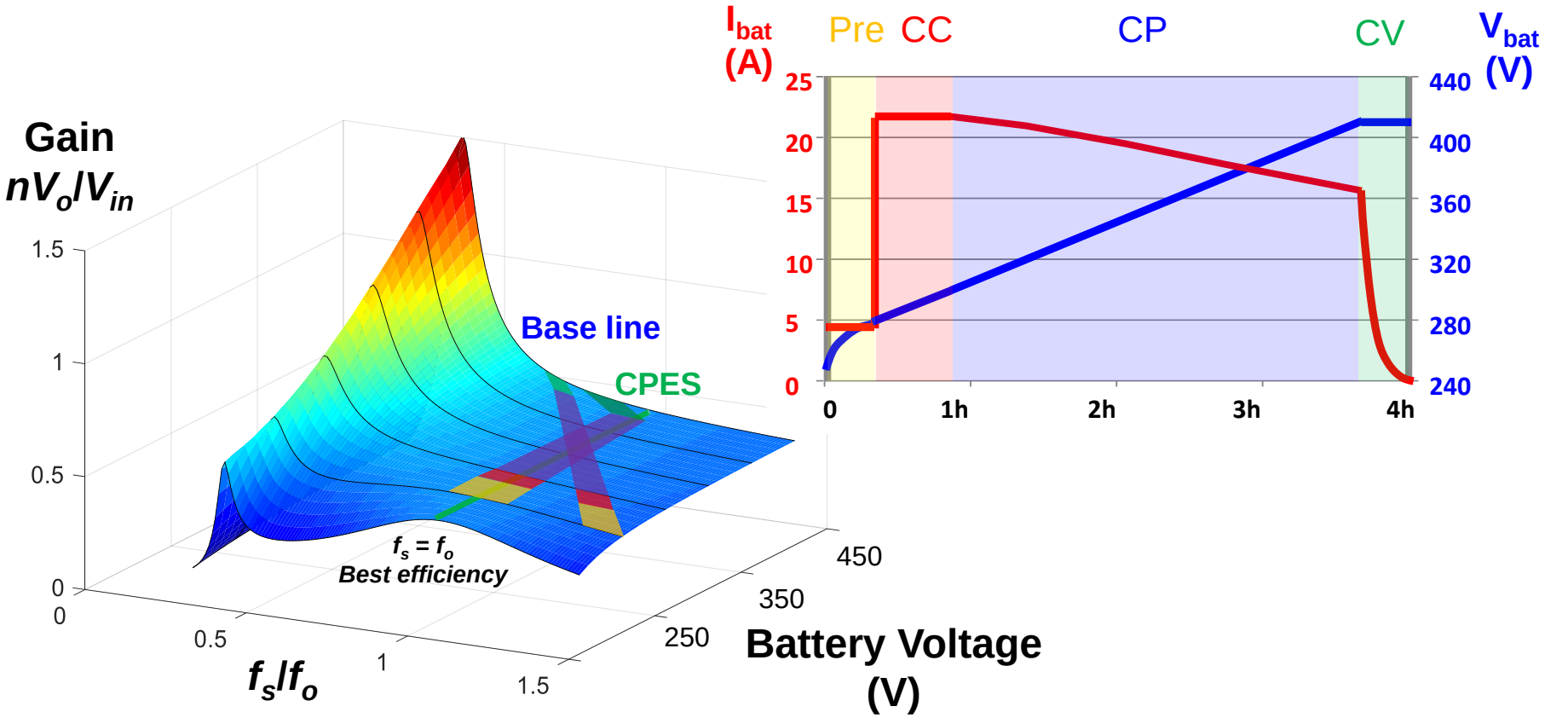
Trade off between DC/DC stage and AC/DC stage

Double Line Frequency Ripple Impact

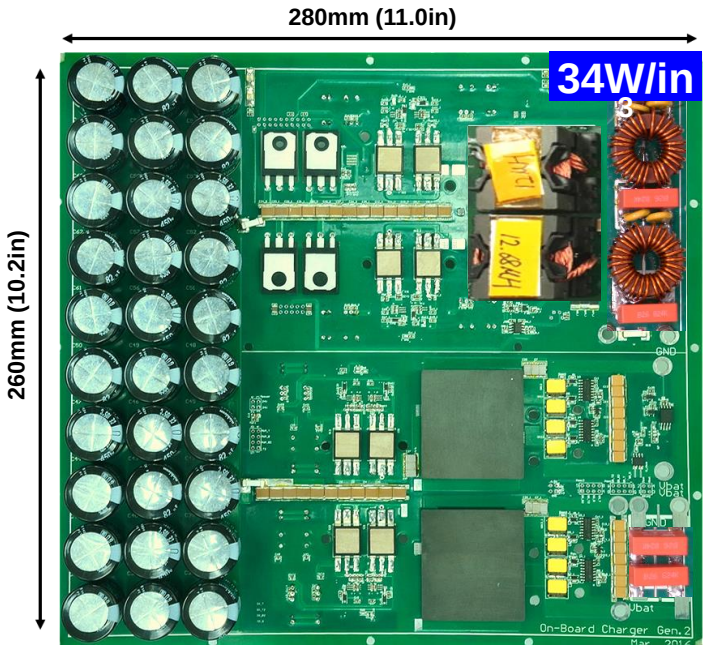




Switching Frequency Range with DC-Link Ripple



Gen. 2 Hardware Prototype and Testing Efficiency



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w/ cold plate

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