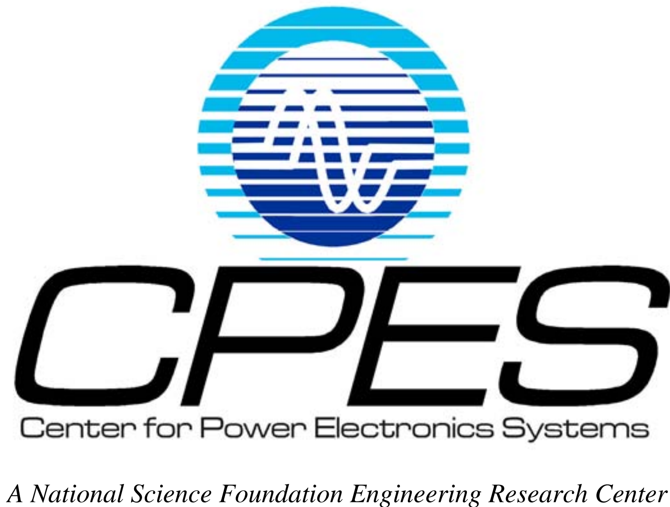


A National Science Foundation Engineering Research Center

Research Program and Facilities Overview

April 2006

Director: Fred C. Lee
Co-Director: Dushan Boroyevich

Virginia Polytechnic Institute and State University
University of Wisconsin – Madison
Rensselaer Polytechnic Institute
University of Puerto Rico – Mayagüez
North Carolina A&T State University

CENTER FOR POWER ELECTRONICS SYSTEMS (CPES)

A National Science Foundation Engineering Research Center

Virginia Tech, University of Wisconsin-Madison, Rensselaer Polytechnic Institute,
North Carolina A&T State University, University of Puerto Rico-Mayagüez

BACKGROUND

Power electronics and related power processing technologies constitute an "enabling infrastructure technology" with a significant potential impact on industrial competitiveness. Power electronics products, to date, are essentially custom-designed, with a long design cycle. Most of the equipment are designed and manufactured using non-standard parts, resulting in a labor-intensive and costly process. With the migration of manufacturing base to Asia, and lately, the outsourcing of engineering and development as well, most power electronics industries are bottom-line focused and emphasize development rather than research. This has led to an increasing concern of the long-term health of the U.S. power electronics industry. At a time like this, U.S. academic researchers must step up their roles and form a stronger alliance with industry, and industry must work with the academics as strategic partners in research and development.

The Center for Power Electronics Systems (CPES) was established as a National Science Foundation Engineering Research Center (NSF ERC) in 1998 with a consortium of 5 universities, including Virginia Tech (VT), University of Wisconsin-Madison (UW), Rensselaer Polytechnic Institute (RPI), North Carolina A&T State University (NCAT), and University of Puerto Rico-Mayagüez (UPRM). The Center's mission is to develop advanced electronic power conversion technologies for efficient electric energy utilization through multidisciplinary engineering research and education in the field of power electronics. The research vision is to enable dramatic improvements in the performance, reliability, and cost-effectiveness of electric energy processing systems by developing an integrated system approach via integrated power electronics modules (IPEM). The envisioned IPEM solution is based on the integration of new generation of devices, innovative circuits and functions in the form of building blocks with standard functionalities and interfaces to facilitate the integration of these building blocks into application-specific system solutions. Furthermore, proposed IPEM approach is deemed quite suitable for automated manufacturing and mass production. Various versions of IPEM have been successfully commercialized, such as, in motor drives and power management solutions for microprocessors.

As a front-runner in power electronics research and with a wealth of talents trained in a multi-disciplinary teaming environment, CPES is uniquely equipped to support the industry efforts. As we prepare for graduation from the 10-year NSF ERC program, we would like to further extend the current multi-university collaboration program to provide leadership through global collaboration to create electric power processing systems of the highest value to society.

CENTER FACTS (1998-present)

- **Research Team:** 32 faculty members and 10 research staff; 63 Ph.D., 44 M.S., and 39 undergraduate students (at present)
- **Industry Consortium:** 80 member firms (at present)
- **Research Funding to Date:** \$26M from NSF and \$40M from industry, government, and institutional supports (Fig. 1)
- **Graduates:** 324 degrees awarded (88 Ph.D., 147 M.S., and 89 B.S.)
- **Publications:** over 1,500 technical papers, theses, and dissertations
- **Technology Transfer:** 40 patents, 12 patents pending, 114 invention disclosures, 129 licenses granted to industry members
- **Education:** 86 power electronics related courses, 27 of which are available for distance-learning access
- **Outreach to Industry:** 51 short courses held; 119 industry internships by CPES students
- **Academic Connectivity:** Collaborative activities with 101 academic institutions worldwide

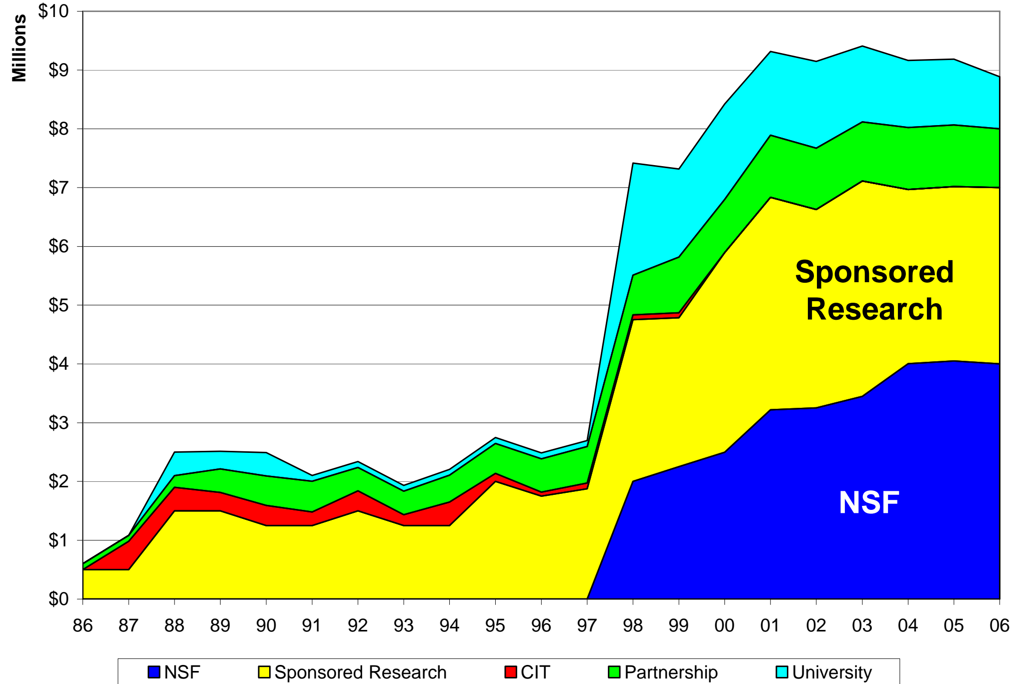


Fig. 1. CPES Funding History.

CPES RESEARCH PROGRAM AND THRUSTS

CPES research focuses on developing innovative power electronics technologies and solutions using an integrated system approach for future electric energy conversion systems. At the heart of our research vision is the concept of the Integrated Power Electronics Modules (IPEM) that can lead to power electronics systems with better performance, higher reliability, lower cost, and reduced development effort. To achieve our research objectives, CPES has assembled a multidisciplinary research team, with expertise covering all aspects of the power electronics. The CPES research program is organized into seven research thrusts, spanned from system technologies, module integration, to advanced packaging and thermal management, and to material and component research. Fig. 2 shows the CPES research thrusts with their leaders.

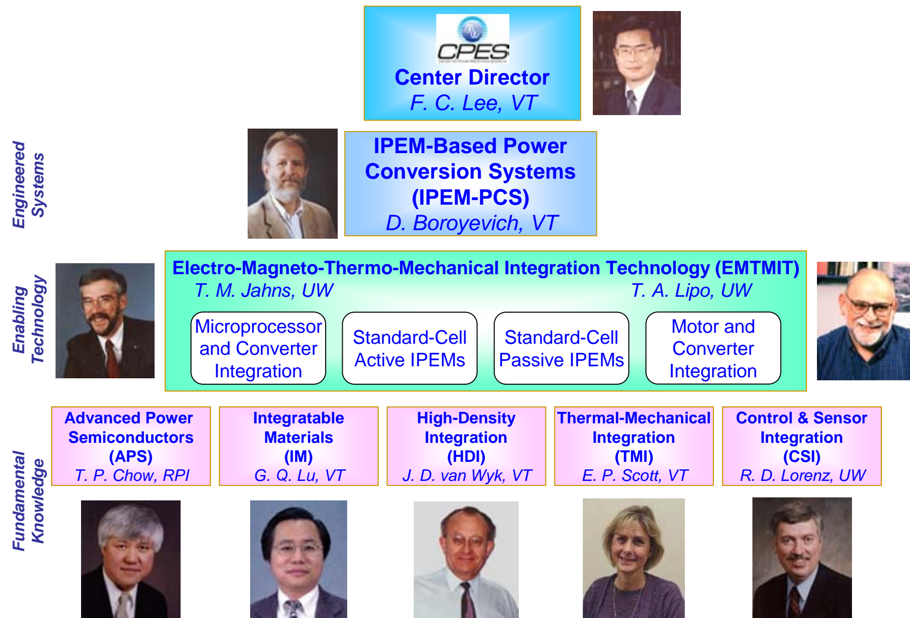


Fig. 2. CPES research program and thrusts.

ENGINEERED SYSTEMS THRUST: IPEM-Based Power Conversion Systems (IPEM-PCS)

The goal of this thrust is to develop an integrated system design approach to the electric energy processing systems based on IPEM and to explore the broader impact of the CPES-developed technologies on the electrical energy usage in our society. The IPEM-PCS thrust is formulated to validate the system integration concept by implementing a complex electronic power distribution test bed using IPEM and IPEM-related technologies developed in other thrusts. The two main **focuses** are: 1) Develop demonstrative converters and system test beds encompassing advanced component, module, and integration technologies from CPES and elsewhere. 2) Develop integrated and generalized methodology and tools for converter system modeling, analysis, design, and optimization. Fig. 3 shows an integrated telecom Distributed Power System (DPS) test bed based on an integrated active switching module (active IPEM), an integrated energy storage passive module (passive IPEM), and an integrated EMI filter (filter IPEM). The integrated converter exhibits a simplified system design and assembly effort, and resulted in significant improvement in performances and power density. Other significant **accomplishments** include the development of an integrated converter design and synthesis methodology combining together the software tools of circuit analysis, circuit and structural layout, electromagnetic analysis and parameter extractions, thermal analysis, and optimization. Currently, an electronics power distribution system test bed is being developed that is representative of wide range of applications, from server farm and data center, to vehicular and alternative energy systems.

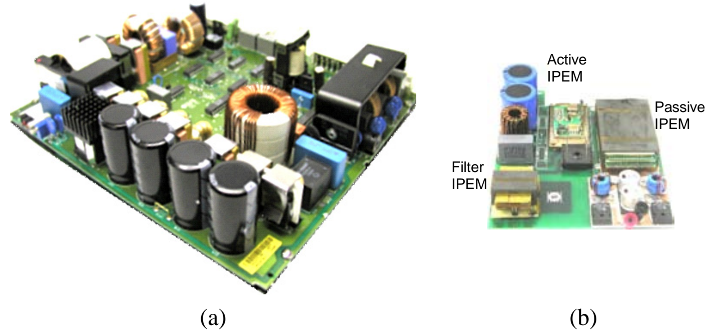


Fig. 3. (a) A state-of-the-art commercial 1kW 48V power converter. 1.5U (1U = 1.75in) profile, 5.8W/in^3; (b) CPES test bed prototype of the same converter, demonstrating six-fold decrease in the number of components and twofold decrease in size. 1U profile, 11.7W/in^3.

ENABLING TECHNOLOGIES THRUST: Electro-Magneto-Thermal-Mechanical Integration (EMTMIT)

The EMTMIT thrust focuses on two aspects of the IPEM. One is the development of integrated modules as a "standard-cell" IPEM and the other is the development of application-specific power electronics integration with loads such as motors and microprocessors. Using mainly the integration technologies from CPES fundamental knowledge thrusts, two basic types of standard IPEMs have been developed in EMTMIT thrust: 1) Active IPEM, which functions as a voltage source single-pole double-throw switch (i.e., a totem-pole half-bridge), integrates two active semiconductor switches, associated diodes, together with gate driver, sensor, protection, and heat transfer structure within the module; 2) Passive IPEM, consisting of integration of energy storage capacitors, inductors, and transformers.

Standard-Cell IPEM (SC-IPEM)

The goal is to develop IPEM technology intended for standard configurations appropriate for use in a wide range of potential applications. Attention is directed towards carrying out proof-of-concept demonstrations that explore the compatibility of new CPES technologies for achieving high performance combined with rugged self-protection features and low cost. Fig. 4 (a) shows a prototype IGBT-based active IPEM using CPES non-wirebond Embedded Power packaging technology.

Integrated Modular Motor Drive (IMMD)

The goal is to achieve significant manufacturability and reliability advantages by developing the integrated motor drive as a modular assembly. A promising approach for achieving this objective is to break the machine stator into individual segmented stator poles with concentrated windings. Fig. 4(b) illustrates the conceptual CPES IMMD that integrates power electronics and controller directly into the motor housing. Rather than simply placing the converter physically close to the motor as done in some commercial products, the IMMD integration is based on a modular configuration – one converter phase-leg per motor pole.

Integrated Power Supplies (IPS)

The goal is to develop the technology needed to achieve a complete physical integration of high-performance power supplies in a three-dimensional multi-chip module. One application example is the integration of such a power supplies with microprocessors to obtain the most efficient power management solution. According to the Intel roadmap, the future generations of microprocessors by 2010 will be well beyond the capabilities of voltage regulator module (VRM) technologies known today, thus a dramatically different approach is required. Fig. 4(c) shows a CPES 3-D IPS module aimed at achieving physical integration of all active and passive components in a 3-dimensional package. The IPS has a multi-coupled cell infrastrcuture with multi-stage multi-MHz multi-phase voltage regulator module (VRM); LTCC resonant converter processing technology for inductors and capacitors; and innovative packaging concepts to enable a System-in-Package (SIP) power module.

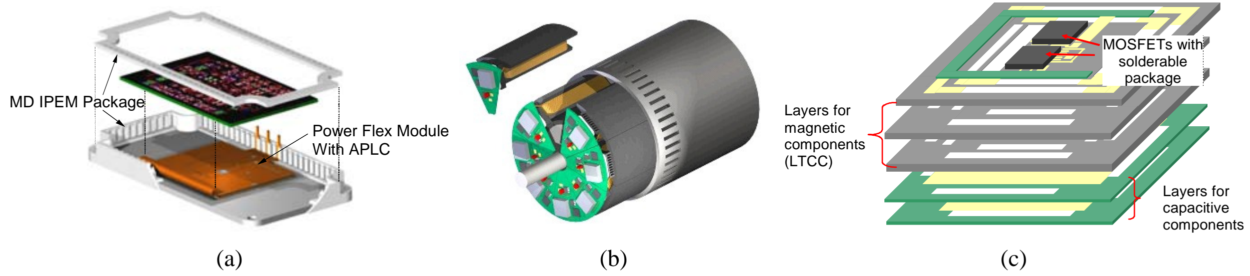


Fig. 4. (a) CPES IGBT active IPEM; (b) CPES integrated modular motor drive; (c) CPES 3-D integrated power supply converter module.

FUNDAMENTAL KNOWLEDGE THRUST 1: Advanced Power Semiconductors (APS)

The goal of the APS thrust is exploration and demonstration of selected novel silicon and wide bandgap semiconductor (SiC and GaN) devices and ICs that will enable significant performance, reliability as well as cost improvements in power electronics systems. We have demonstrated enhancement mode GaN MOSFETs with blocking voltage up to 1kV, by first obtaining much improved MOS properties on GaN capacitors with optimized oxide deposition and annealing conditions. Fig. 5 shows a proposed a GaN MOS-gated bi-directional switch, which consists of a pair of anti-parallel connected complementary MOSFET/Schottky rectifiers. Other significant **accomplishments** include: 1) proposed and demonstrated a novel SiC lateral channel JBS rectifier structure which has low leakage current and capacitance; 2) demonstrated 4kV epi-emitter BJTs in 4H-SiC and performance superior to those of previously reported 3.2kV devices; 3) invented several new Si lateral trench RESURF-type MOSFET structures with overall superior loss characteristics.

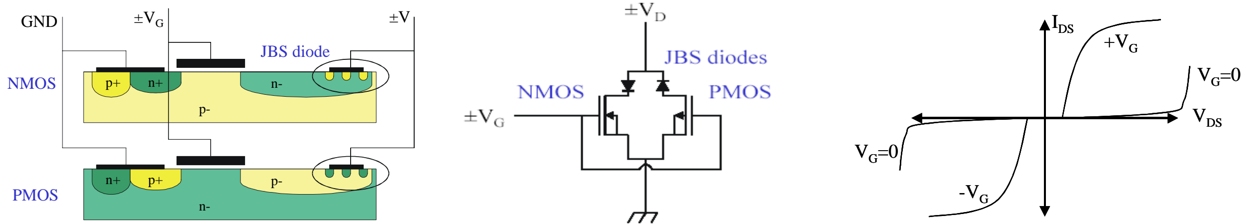
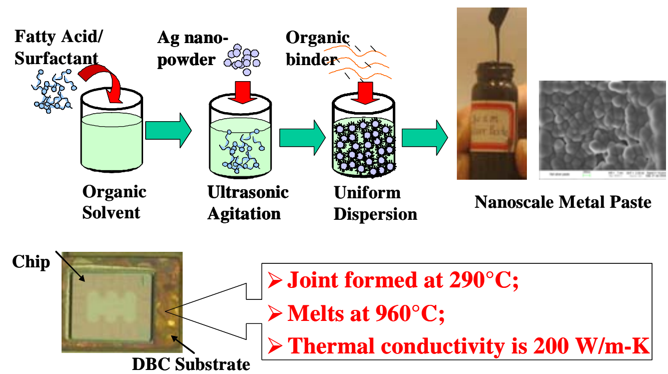


Fig. 5. GaN MOS-gated bidirectional switch: structure, circuit schematic, and characteristics.

FUNDAMENTAL KNOWLEDGE THRUST 2: Integratable Materials (IM)

The goal of the IM thrust is to conduct long-term, high-risk materials research aimed at addressing the needs of four technological areas that are critical to integration of power electronics systems: thermal management; passive integration using multi-functional materials; electromagnetic fields sensing; and understanding physical failure mechanisms. The general technical approach is to explore synthesis, processing, and integration of nanoscale materials that have novel chemical, thermal, and electromagnetic properties. Since its establishment three years ago, the IM thrust has made significant progress in understanding physical mechanisms governing the processing of nanoscale particles and their applications for integration in power electronics systems. Major achievements resulted include: (1) a novel nanoscale

metal paste sintered at low temperature for attaching semiconductor devices; the sintered attachment offers superior electrical, thermal, and thermo-mechanical properties (Fig. 6). The new die-attach solution can also support devices capable of operating at junction temperatures over 500 °C. The technology has been successfully transferred to a start-up company for electronic packaging of



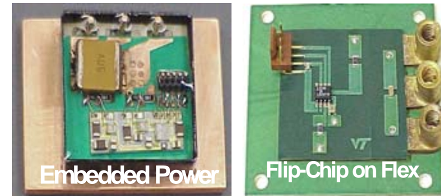


Fig. 6. A lead-free die-attach solution using low-temperature sintering of nanoscale metal paste for high-performance and high-temperature interconnection of semiconductor devices.

microelectronics, power electronics, and optoelectronics devices; (2) synthesis of a multi-ferroic nano-composite for making passive elements; the material system may be used as a platform for integrating passive elements; and (3) fundamental knowledge gained on competing physical processes between coagulation and coalescence aggregation of nano-particles, and its successful application in formulating nanoscale metal pastes for die attachment.

FUNDAMENTAL KNOWLEDGE THRUST 3: High-Density Integration (HDI)

The goal of the HDI thrust is to develop packaging technologies for integrating all the functions in a power electronic converter into modules. The research work in HDI is clustered into three areas: 1) Process technology integration; 2) Module integration technology for designable lifetime; 3) Functional integration of electromagnetic, switching, structural and thermal functions in a power processor module. CPES has been promoting the idea of replacing the conventional wirebond with direct bonding, and has introduced a number of techniques, such as the flip-chip-on-flex and the embedded power technology, as shown in Fig. 8.

Fig. 8. CPES-developed direct bonding technologies.

In 2002, industry followed suit and came out with a range of products that eliminate wirebond, including Fairchild's bottomless and BGA packaging, Hitachi's lead-free packaging (LFPAK), International Rectifier's FlipFet and DirectFET, Siliconix's PowerPAK, and STMicroelectronics FLAT package. In addition, CPES has developed technology for integrating electromagnetic power passives. Fig. 9 shows a passive IPEM that includes four capacitors, two inductors and one power transformer. Functional and process integration with improved thermal management were successfully demonstrated for the first time.

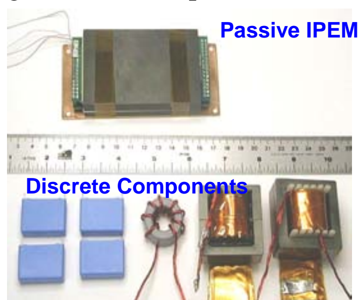


Fig. 9. Passive IPEM vs. discrete components.

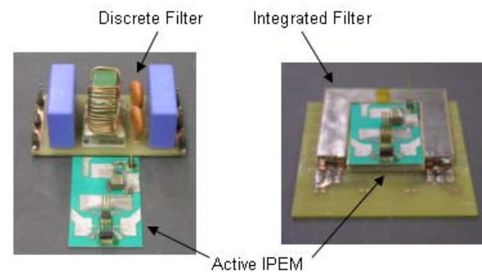


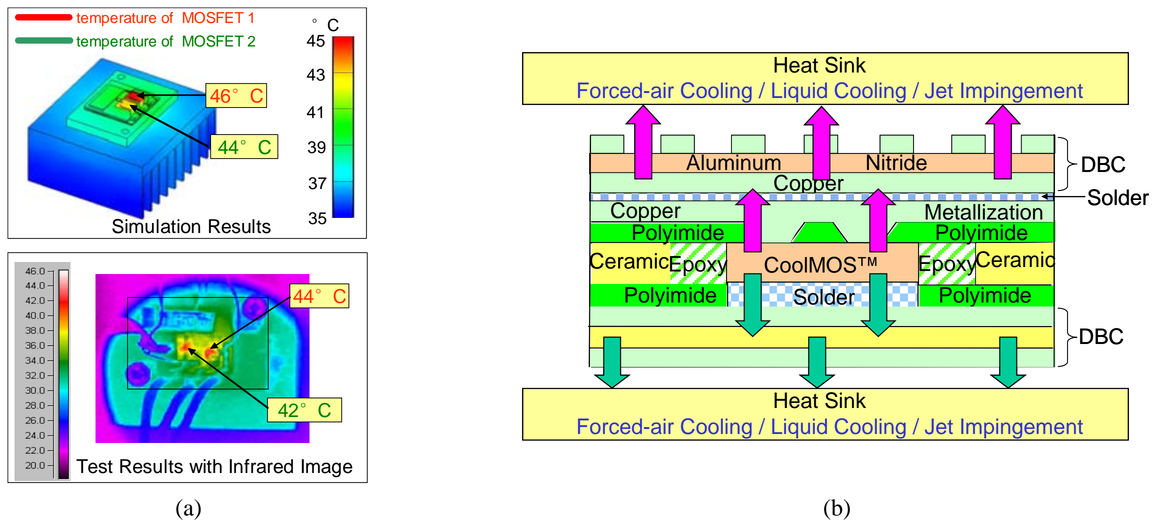
Fig. 10. Integrated filter packaged with active IPEM.

Recently, CPES made a major advance in integrating EMI filters into a low profile, small volume integrated power electronics module (IPEM) with characteristics superior to an EMI filter constructed from discrete components, based on transmission line principles. This filter has already been shown to be effective between 1 MHz and 100 MHz for filtering both common mode and differential mode interference—a range where parasitics are already killing performance of other filters. This new technology will greatly simplify

high frequency interference filters, reduce volume and profile, improve manufacturability, and match perfectly with the planar active IPEM technology (Embedded Power) developed by CPES, as shown in Fig. 10, where the integrated filter is packaged together with an active IPEM.

FUNDAMENTAL KNOWLEDGE THRUST 4: Thermal-Mechanical Integration (TMI)

The overall goal of the TMI thrust is to develop integrated cooling technologies and assess fundamental cooling limitations. The research focuses include the development of 1) multi-level, multi-physical analysis tools and experimental techniques to determine the limitations of performance, 2) integrated thermal management technologies, and 3) methodologies to characterize thermo-mechanical failure mechanisms. Fig. 11(a) shows the active IPEM thermal modeling and test result comparison. Fig. 11(b) shows the concept of integrated double-sided cooling based on the CPES Embedded Power packaging technology, which without using bond wires, allows for the possibility of double-sided cooling by soldering an additional DBC substrate on top of the metallization layer. It was shown that the use of double-sided cooling with heat sinks on both top and bottom substrates improved thermal performance by 62%.



(a) (b)

Fig. 11. (a) Thermal modeling of IPEM; (b) Integrated double-sided cooling based on embedded power packaging.

FUNDAMENTAL KNOWLEDGE THRUST 5: Control and Sensor Integration (CSI)

The goal of the CSI thrust is to create the fundamental knowledge needed to "intelligently" integrate sensors and controls into power electronics with technology approaches that have the potential to significantly improve both functionality and reliability while significantly reducing costs. To achieve this vision, the CSI research **focuses** on three critical aspects: 1) integrated current sensing internal to the IPEM structure, 2) spatial and temporal temperature sensing for load cycle thermal-mechanical stress control, and 3) relative thermal control of parallel IPEMs for robust power sharing. Fig. 12 shows a Giant Magneto-Resistive (GMR) field detection current sensor integrated in an IPEM. GMR temperature sensor was also developed. Other significant **accomplishments** include: active control of switching device junction temperature cycles in power converters to maximize reliability and device utilization; and "sensorless" control of junction temperature differences in parallel-acting power devices to improve reliability.

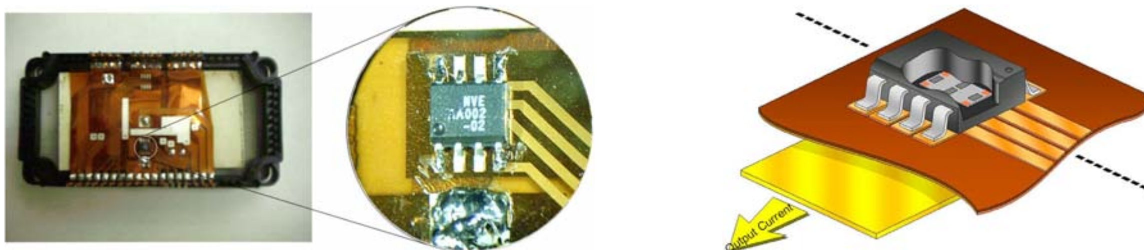


Fig. 12. Using the GMR field detector allows for a simplified compact integrated current sensor design.

TECHNOLOGY TRANSFER AND IMPACTS

Numerous technologies have been produced by CPES through the years, with varying degrees of success in terms of advancing science as well as impact to industry. Prompted by NSF to analyze the Center's technological achievements along these lines, CPES has prepared, in collaboration with the IAB, a two-dimensional chart to identify and illustrate the "low-hanging fruits" generated by the Center. In Fig. 13, technologies identified by thrust leaders to be the most promising emerging technologies are plotted along the X-axis as "Potential of the Center to Lead" and along the Y-axis as "Potential of the Center to Achieve Significant Technology Transfer to Industry/Practitioners". The 28 technologies represented on the chart are analyzed according to their successes and difficulties in terms of technology transfer to industry.

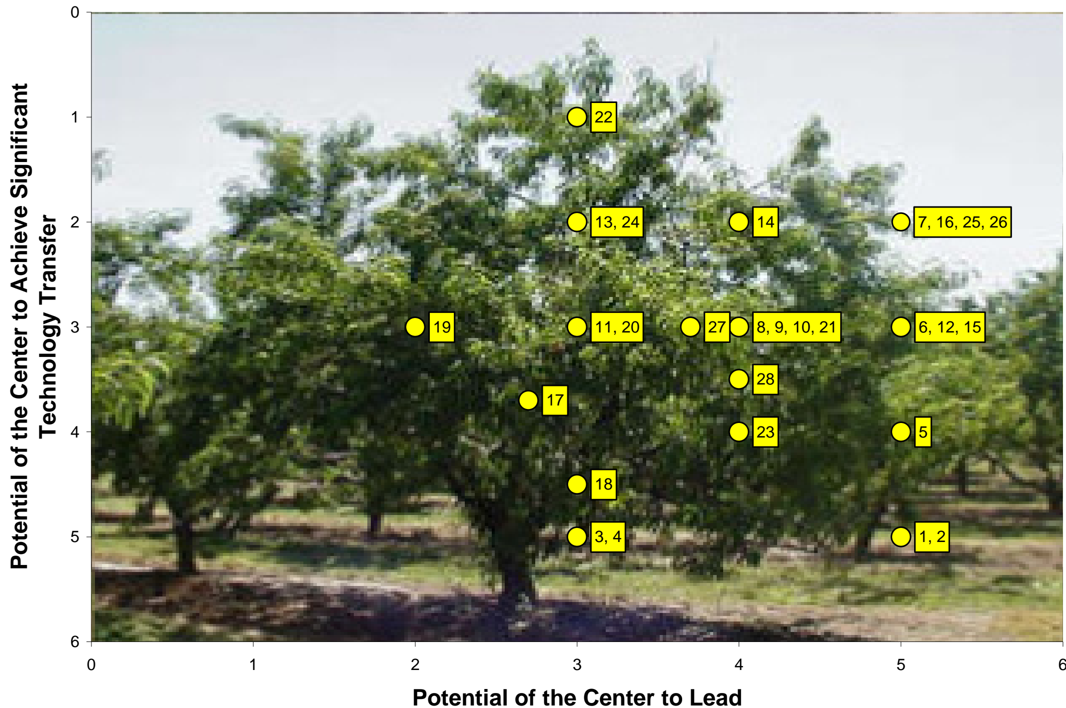


Fig. 13. CPES low-hanging fruits. "Potential of the Center to Lead" is ranked from 1 (incremental impact) to 5 (breakthrough technology), while "Potential to Achieve" is ranked from 1 (technology in idea stage) to 5 (technology is fully mature).

1. Nanoscale material technology for interconnecting semiconductor devices with high heat dissipation and high temperature capability

Successful technology transfer of the low-temperature sintering technique with nanoscale materials for attaching semiconductor devices would enable microelectronics, power electronics, and optoelectronics companies to design and manufacture new products of high performance and reliability. Today all semiconductor devices in the state-of-the-art individual packages or multi-chip power modules are attached to substrates using pastes of lead or lead-free solder alloys or an electrically conductive epoxy. These die-attachments have low electrical and thermal conductivity, and the soldered attachment is susceptible to fatigue failure under cyclic loading. CPES's lead-free nanomaterial attachment possesses better thermal, mechanical, and electrical properties than soldered or epoxied attachment. The low-temperature sintering process is also completely compatible with existing equipment and facilities that use solders or epoxies. Using CPES's material and process, high power-density semiconductor electronic or optoelectronic devices can be operated at high temperatures in excess of 250 °C, not attainable with any existing solder-based die-attach and epoxy materials.

Compared to known die-attach methods, CPES's technology offers:

- Higher performance: because of higher thermal and electrical conductivities.
- Higher temperature capability: melting temperature of the die-attach material is over 900 °C.
- Better reliability: because of tailored thermo-mechanical properties of the attachment.
- Cost competitiveness: low processing temperature and readily available raw materials.

One prominent distinguishing characteristic removes customer acquisition concerns:

- CPES's nanomaterial is a one-to-one replacement for solders or epoxies so that companies do not need to retool their manufacturing processes.

This technology has inspired the founding of NBE Technologies, LLC, a start-up company established by CPES-VT faculty, Prof. Guo-Quan Lu. The company recently received financial support from the Running-Start fund managed by the Corporate Research Center (CRC) of Virginia Tech. With the support, NBE is constructing a production facility in the VT KnowledgeWorks building, a business incubation cradle at the CRC. NBE specializes in the manufacturing of nanoscale materials for electronic packaging and biomedical applications. Its nanoscale die-attach materials are being evaluated by several large manufacturers of power electronics devices and modules.

2. Multiphase buck for point-of-load

Following the 1997 CPES proposal for the multi-phase VRM approach, this technology has now evolved into a multi-billion-dollar industry. Numerous power electronics companies have profited from this CPES IPEM vision and integrated approach. This particular technology has provided U.S. industry the leadership role in both technology and market position. It enables new job creation and job retention in the U.S. Without this technology infusion from CPES, U.S. industry would have lost its market position in providing the power management solutions to the new generation of microprocessors to overseas low-cost providers. This approach has been adopted in many other applications, such as the DC/DC converters for telecommunications, network products, and various forms of distributed power systems (DPS). In the DPS architecture, the single-stage isolated converter is replaced by the two-stage approach. A "bus converter" is used for the first stage to convert 48 V into an intermediate voltage, and the multiphase buck converter was adopted as the post-regulation stage. This architectural change is based on the infrastructure of multiphase buck converter and provides an overall more cost-effective system solution on this sector of industry with a market size even greater than that of the VRM.

3. Current sensing technique for multiphase converters

One of the difficulties of implementing the multiphase buck converter that powers the microprocessor is the issue of current sharing among parallel modules. One of the common techniques for insuring current sharing is to implement some form of current-sensing technique, usually by sensing the inductor current or switch current. However, the conventional implementation of current sensing does not lend itself to easy implementation in a control IC. CPES has developed a patented technology, "A Novel Fast-Transient Response and Minimal-Sized Regulator Modules with Novel Current Sensing and Current Sharing Technology" (U.S. Patent 6,414,469). This proposed approach employs a simple R-C network to emulate the current going through the energy storage inductor, and is very easy to implement in a control IC. This technology has been adopted by such companies as Intersil, ADI, ON Semiconductor, Semtech, Texas Instruments, International Rectifier, Maxim, National Semiconductor, Primarion, etc.

4. Novel Multi-Phase Coupled-inductor and Current Sensing

CPES proposed the coupled inductor concept early in 1999. In the VR application, a large inductance is preferred for steady-state operation, so that the current ripple can be reduced. However, for the transient response, a small inductance is preferred so that a high transient inductor current slew rate can be achieved. This conflict can be resolved by using the coupled inductor. When the inductors are coupled in a multi-phase buck converter, by virtue of the switching network, the coupled inductors behave like non-linear inductors. The equivalent inductor is large for steady state and small for transients. This concept from CPES is being adopted by two companies, Volterra and Advanced Energy (AE), with their specific implementations patented. Their implementations, although attractive, are not without limitations. Volterra's coupled inductors utilize an excessively long winding path, and AE's implementation uses a multi-core approach. CPES has developed another alternative coupling implementation that circumvents their IPs and realizes improved performance at the same time (VTIP 05.040, VTIP 05.063).

With the coupled inductor, the prevalent DCR current sensing method in current non-coupled inductors does not apply anymore. To solve this issue, CPES also proposed a novel DCR current sensing network for the coupled inductor (VTIP 05.064). These three invention disclosures have been approved by the IPPF members for patent applications.

5. Change in distributed power architecture and eliminate the use of highly customized front-end DC-DC converters with multiple outputs by a bus converter single or dual outputs

As the Intermediate Bus Architecture (IBA) is prevalent in the server and telecom applications, the intermediate bus converter (IBC) has become one of the hottest products. CPES has developed several high-density IBC technologies (VTIP 03.115). The advantages can be summarized as follows: no output inductor, ZVZCS for all devices and no body diode loss. Our prototype hardware has demonstrated 500 W output power in a quarter brick size. Compared with industry practice, its power density is about 3 times higher.

Encouraged by the success of the 48 V two-stage architecture in the server and telecom application, CPES is also investigating the 400 V to 48/12 V bus converter for the future high-end applications by adopting the LLC resonant technology. So far, 1 MHz, 1 kW semi-regulated LLC resonant bus converter is being developed for the architecture.

Currently, the front-end of the DPS is realized by a highly customized design with multiple outputs. Engineers are reluctant to change to a simplified distributed power architecture with a bus converter unless the proof-of-concept prototype is demonstrated with verified performance improvement and cost-savings. The difficulty is that cost-saving needs to be demonstrated with economy of scale. Nevertheless, companies such as Intel, IBM, and HP are pushing the change of distributed power architecture in this manner. Therefore, it is anticipated that this approach will be adopted in the near future.

6. Digital control in power supply applications

In recent years, the interest in digital control for switching converters has grown considerably. The digital control approach potentially offers several advantages compared to the analog counterpart, such as the immunity to component variation, the ability to perform sophisticated control algorithm, and self-calibrations, faster IC design using HDL synthesis and controller adaptation. In spite of these potential advantages, one of the limiting factors when using IC digital controller in high-frequency switched-mode power supplies (SMPS) is the achievement of dynamic performance comparable to those of analog controllers, especially in the presence of significant control delays and quantization effect. Thus, one of the major challenges in digital control for SMPS is the development of simple digital or mixed-signal control architectures with no silicon area required which ensures dynamic performances comparable to analog controllers. Such a controller usually requires high-resolution analog-to-digital conversion and digital-pulse-width modulation (DPWM). The IC implementation of such a control is usually complex. It is also hampered by the undesirable quantization effect and limit cycle oscillation. Researchers at CPES have developed a novel DPWM method that could achieve a resolution approximately 10 times greater than conventional DPWM methods. The design challenge of DPWM block could also be greatly reduced. We are currently discussing this concept with industry partners and a potential user—Primarion—for possible implementation in their commercial digital control IC.

7. A complete (3-D) integration of power supply (integration of both active and passive components) for non-isolated point-of-load applications that extended up to 50-100 Watt applications

One of the major reasons for the successful deployment of multiphase VR for microprocessor applications is its simplicity, modularity, and scalability. Furthermore, an infrastructure for supporting this multi-billion-dollar industry is already in place to provide cost-effective solutions for a wide range of applications. Recently, Enpirion introduced a new product with 6 A, 0.8~3.3 V. The limitation for such a product is the ability to integrate inductors on a silicon substrate. The technology CPES developed uses low-temperature co-fired ceramics (LTCC). Researchers have successfully built inductors using LTCC, and are at present investigating making capacitors. LTCC technology enables the integration of low-profile inductors with much higher current capabilities. The Center has also successfully packaged low-voltage devices using embedded power technologies in a recent prototype.

Such an aggressive approach of high-level integration at high-power level presents inherent risk, especially when integrating multiple high-risk technologies. The long-term reliability of LTCC technology, when applied to high power applications, although demonstrated successfully in the lab, is yet to be established. Finally, the optimization of the entire module layout for SIP (System in Packaging) requires knowledge of a breathtaking number of interrelationships.

8. Integrated magnetics and dielectrics for 100 kHz – 10 MHz EMI filter

Researchers in the HDI thrust have pioneered an integrated EMI filter with significant reduction in parasitic inductance of filter capacitors, reduction of undesired mutual component couplings, and reduction of winding capacitance of the inductor. The internal electromagnetic parameters in the three-dimensional integrated structure can be controlled to enhance the attenuation of high-frequency noise. This is done through the use of different interleaved materials and a three-dimensional geometrical configuration in order to cancel the undesired electrical field coupling to achieve near ideal behavior in the frequency band of interest. The integrated EMI filters have been demonstrated to be superior to their discrete counterparts in terms of filter behavior, profile, and power density. In addition, the concept of a broadband EMI filter, by incorporating transmission line filters with the previously developed filter IPEM into one structure, surfaces as a major breakthrough during the past year. This now enables the construction of a filter IPEM with a cut-off band from around 100 kHz to 100 MHz. In order for this technology to be commercialized, the reliability of this integrated EMI filter needs to be studied thoroughly before final adoption by industry.

9. Integrated resonator and transformer for resonant power supply

The HDI thrust has developed technology for integrating electromagnetic power passives. This passive IPEM replaces the functions of discrete capacitors, inductors, and power transformers. The passive integration is built upon multi-layer, three-dimensional structures utilizing materials with different properties such as high permeability, high dielectric constant, and high conductivity, in order to achieve integrated multi-functional properties. Functional and process integration with improved thermal management was successfully demonstrated in the lab for the first time. The original breakthrough of integrating electromagnetic power passives containing inductors, capacitors, and transformers has led to the developed CPES technology for passive IPEMs and EMI filter IPEMs. In order for this technology to be commercialized, a long-term reliability study of integrated passive IPEMs should be thoroughly studied before final deployment in the form of a commercial product.

10. EMI filter (1 MHz – 100 MHz) using integrated transmission lines

CPES has now booked a major breakthrough by pioneering a completely new type of filter based on transmission line principles. This filter has already been shown to be effective between 1 MHz and 100 MHz for filtering both common-mode and differential-mode interference—a range where parasitics are already killing performance of other filters. The filter consists of transmission line absorbing elements stacked between the bus bars feeding the active power electronics module (IPEM). The filter thus avoids the first disadvantage of the "classic" generation, since it only handles the small absorbed interference power—a negligible fraction of the main power. The total system power passes through the bus bars around the filter. The second disadvantage based on the effect of parasitics is avoided, since as the frequency increases, the absorber works better as a transmission line, improving the absorption.

11. Embedded Power technology for fabricating modules integrating switching devices, sensors, gate drivers, and passives for motor drives

CPES has successfully implemented Embedded Power to succeed the previously used Flip-Chip-on-Flex technology to develop an active IPEM for motor drive application. Several CPES technology advances are being incorporated into the active SC-IPEM design. Embedded power technology has been adopted to eliminate all wire bonds in favor of a planar interconnection scheme that minimizes dangerous voltage transients caused by undesired parasitic inductances. In addition, the flat upper surface is valuable for mounting gate drives, sensors, and cooling components to extract extra heat from the top side of the module. Such advances contribute to reducing the module size while increasing its long-term robustness. This technology also provides valuable opportunities for combining active gate drive including adjustable dv/dt control and self-boost charge pump for the high-side gate drive power supply, and isolated GMR sensors for combined current and thermal sensing. These features will result in higher power module robustness and reliability that are key attributes desired by both the manufacturers and users of these modules.

12. Inversion Mode GaN MOSFET Technology

We have demonstrated the world's best ion-implanted, enhancement mode, n-channel GaN MOSFETs on p and n GaN epi on sapphire substrates. The maximum field-effect mobility of 167 cm2/V-s, minimum subthreshold slope of 170 mV/decade and blocking voltage up to 1 kV have been measured. The much-

improved MOS properties were first obtained on GaN capacitors with optimized oxide deposition and annealing conditions. We have discovered that the interface state densities are much lower near the conduction band edge than those near the valence band in GaN, quite different from those in Si and 4H-SiC. This trend also implies that it is more difficult to demonstrate p-channel devices than n-channel devices. Furthermore, our progress in n-channel MOSFET is a major step forward on the ultimate demonstration of high-voltage MOS-gated bidirectional switch in GaN. As this is still in experimental stage, further development of a proof-of-concept prototype is necessary before commercialization is possible.

13. Single phase motor drive with reduced switch count

Research on motor drives has generated new inverter topologies for single-phase induction motors that reduce the switch count to as few as two, providing the basis for fractional-horsepower HVAC motor drives with reduced cost and higher reliability.

14. Axial flux permanent magnet machine with field-weakening capability

Research on modular permanent magnet motors has led to a new concept for a small, flat motor that is an attractive candidate for application in computer disc drives. The motor has an axial-flux configuration that evolved from a radial-flux design distinguished by its use of sinusoidal-shaped stator pole faces. When this pole shaping is converted into an axial-flux design, the stator poles take on a “flower petal” shape. Since the poles are linked with a sinusoidal flux emanating from the rotor permanent magnets, the torque produced by the machine can be nearly constant. The topology is compatible with high-volume manufacturing and has fewer parts than the disc drive motor commonly used today. A patent is being filed on this concept.

15. Active Standard-Cell IPEMs consisting of inverter phase legs that incorporate planar interconnect packaging, integrated current sensing, active control of switch dv/dt, and dead-time elimination

During the last several years since CPES began, major progress has been demonstrated in the development of advanced IPEM using flip-chip-on-flex circuit planar interconnect technology. It shows significant promise for improving the performance of future generations of commercial power modules. This has been confirmed by recent feedback from CPES industrial sponsors, who recognize the potential value of these features. There are also clear signs in new power module product offerings that trends toward higher levels of feature integration are continuing and perhaps even accelerating.

However, the rate of this technology transfer process has been slowed by power electronics design engineers who are hesitant to give up their ability to supply their own fully customized gate drive, sensor, and protection functions in order to purchase integrated power modules that provide these advanced features in standardized combinations. There is also concern about the long-term reliability of these new integrated features based on historical problems with early generations of power-IC gate drive chips that predate CPES, but still live on in the memories of some customers. Successes with new generations of power modules that include advanced features are gradually overcoming these obstacles to immediate customer acceptance, but engineering conservatism and high component cost sensitivity continue to constrain the rate of IPEM technology penetration.

16. Integrated Modular Motor Drive (IMMD) configuration that is assembled from modular phase-drive units, each including a motor pole, its winding, and inverter phase-leg

The Integrated Modular Motor Drive (IMMD) represents an exciting concept for future motor drives that combines the appealing characteristics of load-converter integration with the advantages of modularity for low manufacturing cost and high fault tolerance. According to this concept, the basic building block of the IMMD machine consists of an iron pole piece with a simple concentrated coil wrapped around it, together with its dedicated phase-leg controller that includes both the power electronics inverter and a digital signal processor (DSP).

There are clear indications that industry is already moving to introduce integrated motor drive products into the marketplace, but this IMMD concept contains several advanced features that are delaying the technology transfer process. In particular, the integration of the controller into the machine housing places higher-than-normal thermal stresses on the electronics. As a result, the development of IMMD products will benefit greatly from the future availability of high-temperature electronics components such as silicon carbide (SiC) power devices that are just beginning to appear in the marketplace.

In addition, motor drive customers are suspicious of the long-term reliability characteristics of power electronics when it is embedded inside the machine. As a result, market acceptance of the IMMD concept depends on the successful development of high-temperature, high-reliability power electronics that is being pursued by researchers both inside and outside of the CPES universities for use in a wide range of applications.

17. Converter design optimization using genetic algorithm

This technology represents more new methodology for design than it enables specific new products. The only real product that could be developed based on this technology is design software. The proposed ideas and concepts already have found their way into new products by local start-up companies, such as Adoptech and Phoenix Integration, and they are affecting technology roadmaps of some of the larger industrial partners. In that sense, the technology transfer has been already happening, although the level of maturity is 3.7 out of 5. Further development of the technology within CPES, to the level 5, would be probably a waste of resources because the industry would never use it in unchanged form anyway.

18. Improved double-sided and integrated microchannel cooling for IPEM structures

The use of embedded power allows for the possibility of double-sided cooling, in which an additional DBC substrate is soldered on top of the metallization layer. The DBC provides electrical isolation as well as a good heat path. Combinations of the ceramic materials that can be used for the DBC substrate, along with other commercial substrates such as Thermal Clad™ and ALOX™, were numerically investigated to improve thermal performance. Other methods to further improve thermal management include the integration of microchannel cooling. The numerical results show that the use of double-sided cooling can improve thermal performance by at least 30%. Although the use of Thermal Clad™ as the top substrate can improve the thermal performance by 36%, an aluminum nitride DBC ceramic provides an additional five percent enhancement over the Thermal Clad™. Significant improvement was found with the inclusion of microchannel cooling in the top polyimide layer of an Insulated Gate Bipolar Transistor (IGBT) IPEM even without the added DBC layer. Integrated micro-channels located specifically over localized hot spots provided a 29% decrease in the maximum temperature rise of the IPEM above the ambient. Experimental investigations were also conducted to demonstrate the benefits of double-sided cooling. It was shown that the use of double-sided cooling with heat sinks on both top and bottom substrates improved thermal performance by 62%. These studies have demonstrated the tremendous benefits of embedded power by enabling the use of double-sided and integrated microchannel cooling. Furthermore, it has been demonstrated that these technologies offer the possibilities for further enhancement through structural modification and material selection.

19. Multi-ferroic composite serving as a multifunctional substrate for monolithic integration of capacitive and magnetic elements

Multi-ferroic composite materials are artificially designed and synthesized to have tailorable dielectric and magnetic properties such that capacitive and magnetic elements can be fabricated on the same material platform. Successful transfer of this technology would enable manufacturers of electronic products to shrink the size and weight of passive components in an electronic system, reduce the fabrication complexity, and potentially lower cost. In today's power electronics packages and modules, passive components such as inductors and capacitors tend to be bulky because of the requirement that they must be able to handle large amounts of energy, and therefore take up a disproportionate amount of real estate on the mounting substrate. The existing method of integrating passives involves assembling separate layers of ferroelectric materials (e.g., barium titanate) with high dielectric constant (high-κ) for the electrostatic energy storage, and a ferrite core having high magnetic permeability (high-μ) for the magnetic function. This imposes physical, mechanical, and processing limitations, while not substantially contributing to volume reduction. Thus, advances that can miniaturize passives, as enabled by CPES's multi-ferroic composite technology, will lead to significant reduction in the size and weight of electronic products.

However, successful transfer of CPES's multi-ferroic composite technology faces enormous challenges. For one, there are still many unanswered scientific questions concerning design, synthesis, and fabrication of multi-ferroic materials because of a combination of synthesis and processing issues and application requirements having competing demands. Lack of in-depth understanding on the fundamentals of these

materials hampers the development of material systems with optimized multifunctional properties to meet specific application needs. The second challenge facing the successful technology transfer comes from the generally slow acceptance by system engineers to new materials or device technologies. This may be because the adaptation of a new materials/component technology would require rethinking of system-level designs to fully realize the advantages and opportunities presented by the new technology.

20. 3D Integration Process based on low-temperature co-fired ceramic for realizing integrated power supplies

Low Temperature Co-fired Ceramics (LTCC) technology is widely used in RF and microwave applications. However, the existing process of screen printing the conductor paste on green tapes makes it unfavorable for power electronics applications. The process is being modified to incorporate thick conductors in the green tapes, to improve the current carrying capability of the embedded conductors. Power inductors have been fabricated using the modified process and tested up to 16 A, while maintaining the profile of the embedded inductor to less than 1 mm. The modified process has allowed the use of LTCC technology for power electronics applications. In addition, the low profile of the embedded passives fabricated using this technology allows integration with active devices to form an integrated modular system. The thermal performance is also expected to be improved with the planarity of the module. Since this material is only recently commercially available, the LTCC process of making integrated power supply with integrated magnetics and capacitors in the packaging substrate is highly doable and presents no obstacle for commercialization. When the economy of scale is reached, the cost of the green tape material will come down dramatically, making this a cost-effective solution.

21. SiC LC-JBS Rectifier

Present commercial high-voltage SiC Schottky rectifiers have a delicate tradeoff between forward voltage drop and leakage current density at elevated temperatures. By employing an epitaxial re-growth over p+ implanted buried regions to realize shielded Schottky junction regions, researchers have demonstrated advanced 1 kV SiC Schottky rectifiers with leakage current density as low as that of SiC pin junction rectifiers, with a minimal (about 0.2 V) increase in forward drop. While unit cell design has been optimized, technology transfer of these rectifiers to manufacturing requires process simplification and sensitivity assessment, which will be accomplished by interacting closely with interested industrial partners.

22. Axial flux machine using soft magnetic composite materials

Generated from ongoing research at UW, this work explores the use of soft magnetic composite (SMC) materials both as a replacement to steel laminations and as the core material in new electromagnetic actuator topologies. This project aims to benefit: 1) powder-producing companies by providing verification to their in-house test results as well as a better understanding of the different material properties required by different motor topologies; 2) powder compaction companies by providing methods for analyzing SMC characteristics accurately and effectively for quality control and processing improvements; 3) SMC motor manufacturers by providing the in-depth JMAG analysis methodology for losses which will be crucial for motor design enhancements. However, in order for industry to adopt it for commercialization, different methodologies for modeling material losses in SMCs and a proof-of-concept prototype need to be further investigated.

23. IGBTs and monolithic IGBT/diodes with pilot current sensors, including control techniques for using them to achieve high-performance current regulation in AC motor drives

Pilot current sensors have been successfully integrated into both IGBTs as well as the accompanying anti-parallel rectifier in a monolithic device. Techniques have been demonstrated experimentally for delivering high-performance sinusoidal current regulation for motor drives using incomplete current feedback measurements provided by integrated pilot current sensors installed only in the low-side inverter switches. Currently, researchers are proceeding with a small number of pilot runs of these devices to be utilized later on for a proof-of-concept prototype before final deployment for commercialization.

24. Distributed control architecture for IMMD that coordinates all of the independent phase-leg controllers, providing robust control properties and fault tolerance

A new architecture has been pioneered for future AC machine drives known as Integrated Modular Motor Drives (IMMDs) that takes drive integration concepts to a new level by integrating the power electronics and controller directly into the motor housing. Modularity is given particular emphasis in this

architecture by segmenting the motor stator into N individual pole pieces with compact concentrated windings, each of which is mated with its own independent power converter and controller. These integrated motor pole units provide long-term opportunities for cost reduction by standardizing the motor drive building blocks, as well as increased reliability by offering attractive opportunities for fault-tolerant operation following failure of one of the N pole units. Currently, CPES is in the process of developing a proof-of-concept prototype using the concept. This technology will not be ready until Year 10.

25. Giant magneto-resistive (GMR) current sensors integrated inside IPEMs to provide both high-bandwidth current feedback and semiconductor switch temperature readings

The use of point field detectors (giant magneto-resistive, or GMR) for integrated current sensing was advanced significantly in 2005 by developing optimization methods for which show the promise of yielding MHz bandwidth sensors of extremely high linearity for the most practical interconnect bussing structures. The GMR detectors serve the dual purposes of high fidelity, isolated current sensing while simultaneously sensing the internal IPEM temperature in close physical proximity to the power devices.

26. Maximizing reliability and device utilization via sensing and control of junction temperature in power converters

CPES's control and sensor integration activities have developed several control and sensing techniques to improve reliability by actively limiting thermal-mechanical stress.

The active control techniques have focused on two major issues. One is focused on limiting power cycle induced ΔT_j thermal stresses. The second is focused on sharing relative thermal stresses uniformly between load-sharing power devices and converters.

The integrated sensing techniques have focused on using intrinsic bus ringing signals to estimate junction temperature. The information is also intrinsically communicated on the power bus. The combined effect is to enable relative temperature control without additional sensors and communication equipment. Patent applications for this technology were made in October of 2005.

The basic CPES research for all of these technologies has been actively tracked via visits by industry, but the development projects needed to get this technology into products are largely occurring independently in the individual firms.

27. Multi-disciplinary software integration for solid body based mechanical, thermal, electromagnetic, and electrical design of power electronics modules and converters

CPES promoted an integrated design methodology for power converters combining commercial software for circuits, electromagnetics, thermal, structural, and system optimization within a unified environment, which greatly enhances power electronics research and development capability as well as drastically reducing design and analysis cycles. Software packages such as I-DEAS™, Maxwell 3D, and Saber™ can be linked together for a multi-disciplinary design. This concept has been adopted and furthered by Ansoft, which now offers the comprehensive set of integrated software packages including Maxwell® for electromagnetic and electromechanical analysis; Simplorer® for circuit-based time- and frequency-domain analysis, block diagram, and state machine simulation languages; and ePhysics™ for thermal and stress analysis, with the use of RMxprt™ and PExprt™ for electrical machine and magnetic component design respectively.

28. Modular and hierarchical modeling of electronic power distribution systems for system architecture design and optimization with respect to size, efficiency, and reliability

CPES has promoted a hierarchical modeling and simulation approach, encompassing thermal, electrical fundamental (average), medium frequency (ripple, harmonics), and high frequency (EMI) sub-models for the design and analysis of IPEM-based power conversion systems. This modeling and simulation vision has exploited the IPEM concept by taking advantage of its inherent scalability, modularity, and reconfiguration capability and applying it to the system analysis and design. CPES has promoted this modeling approach through ONR in the past and recently through its NSF ERC IPEM-PCS thrust. As a result, industry and academia pursuing similar fields of studies have embraced and benefited from this methodology. Affected companies include ABB, F&H Applied Sciences Associates, Northrop Grumman, L3, Thales, Hamilton Sundstrand, Boeing, BAE, etc.

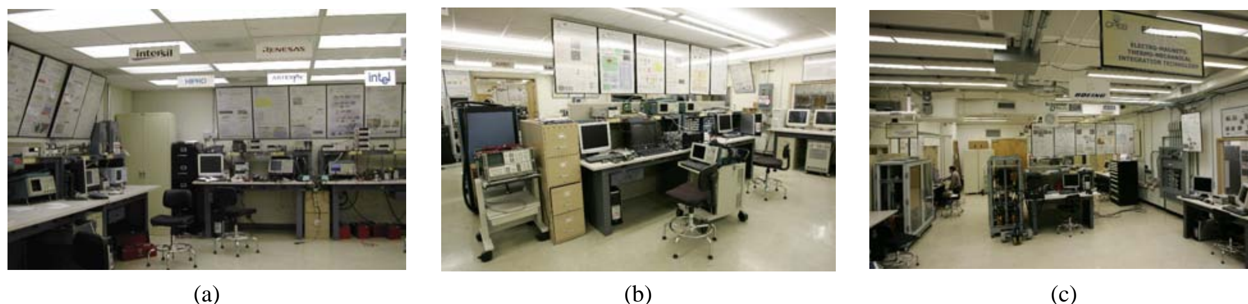
APPENDIX

RESEARCH FACILITIES

Virginia Tech

The CPES power electronics lab at Virginia Tech is among the largest and best equipped university labs in the world. It occupies over 13,000 sq. ft. space, and houses a Power Electronics Research Lab, an Integrated Packaging Lab and a Computational Lab. These labs are equipped with state-of-the-art power testing equipment, dynamometers, prototype PWB manufacturing equipment, an EMI chamber, a clean room, a mechanical shop, and numerous high-end computer workstations.

The Power Electronics Research Lab is equipped with state-of-the-art tools and instrumentation necessary for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6kV, 1MW. Standard instrumentation is comprised of GHz oscilloscopes; function generators; network, spectrum, impedance, logic and power analyzers; thermal sensors; and AC/DC bench supplies of all sizes. Specialized equipment includes: thermal test equipment; Hi-Pot tester; 3-D magnetic field scanner; EMI/EMC analyzer; large and small dynamometers; automatic circuit board routing equipment; programmable and variable loads; and liquid cooled heat-exchanger. Fig. A-1 shows snapshots of the lab including the state-of-the-art high-power medium-voltage setup under construction. CPES at Virginia Tech will be one of the few universities with testing capability up to 1MW, 4kV AC and 6kV DC.



(a) (b) (c)

Fig. A-2. CPES VT power electronics research labs: (a) low power lab; (b) medium power lab; (c) high power lab.

The Integrated Packaging Lab, as shown in Fig. A-2, is the only university facility in the nation devoted to power electronics packaging research. It has the capability to produce FR4, DBC, and thick film hybrid substrates, mount bare die and SMT components, and perform thin film deposition, metal plating, ceramic laser machining, and device wire bonding. Component and module level thermal measurement, environmental and electrical testing capabilities, including device die probing and inspection via microscope, are also available.

Fig. A-2. CPES VT Integrated Packaging Lab.

The Computer Lab supports all major software used in power electronics analysis and design, including: SPICE, SABER, PSCAD/EMTDC, I-DEAS, Analogy Design Tools Workbench, Ansoft-Maxwell 2-D and 3-D finite element analyzers, Mentor Graphics and Cadence circuit simulation software, Simplis, TMA, Flotherm circuit thermal analyzer software, Silvaco device simulation software, iSIGHT, and Ansys.

University of Wisconsin-Madison

The lab is equipped for 50-60 graduate students to work on machines, motor drives, power electronics circuits, and machine and power electronics packaging research. For machines and motor drives, there are with eleven machine bases and a range of dynamometers up to 50 hp, including numerous units designed for high speed testing.

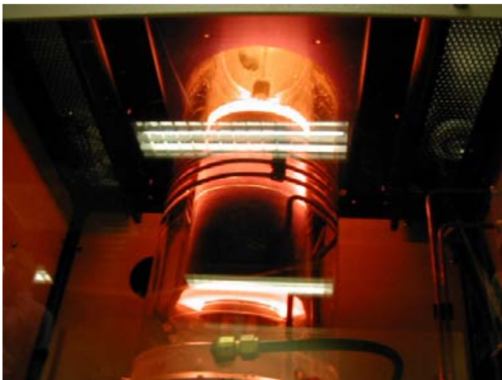
For high voltage power converters, there are two high voltage cages suitable for medium voltage operation. A variety of commercial and specially constructed power converters and DSP-based controllers are available for general drives and power converter research activities. Printed circuit board assembly/disassembly equipment includes a pick-and-place machine, a solder reflow oven, inspection microscope, and a variety of current technology soldering and de-soldering equipment. A large range of test and measurement instruments needed for power electronics and machines research are available in the lab, including thirty LeCroy and Agilent digital oscilloscopes, sixty differential voltage probes, and a correspondingly high number of current probes. Also installed is a 36 cubic feet Envirotronics environmental chamber, which allows testing from -73 to +177 °C. Complementing this chamber is a Flir real time infrared temperature measurement camera system. The power distribution system, workstations, switchgear, test equipment, and wiring infrastructure of the laboratory are configured with a lab-wide bus work allowing clutter free electrical interconnection between workstations. Power available in the lab includes: 480V three-phase AC; 208V four-wire three-phase AC; 230V three-phase AC, and 230V DC. Fig. A-3 shows a medium voltage test rack in the lab.

Fig. A-3. A medium voltage test rack in the University of Wisconsin lab.

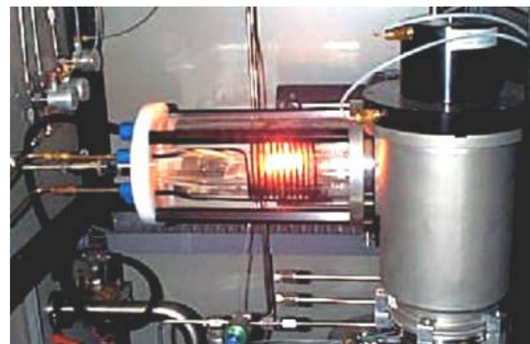
Rensselaer Polytechnic Institute

RPI has well-equipped facilities for materials characterization, processing and device fabrication research. Key central facilities include: a class 100 microelectronics clean room (MCR) for semiconductor processing and device fabrication, electron microprobe x-ray analysis (EDAX or EPMA). Key facilities in CPES lab include one low-pressure horizontal cold-wall reactor [Fig. A-4(a)] dedicated to grow p-type and n-type SiC films, and another vertical hotwall SiC reactor [Fig. A-4(b)] that is suited to grow thick (>100μ), low-doped epitaxial films. Other facilities to characterize materials include a double crystal X-ray diffractometer, variable temperature and variable magnetic field Hall measurement system, Fourier transform infrared (FTIR) spectrometer, low temperature PL system as well as C-V and I-V measurement system. A spectroscopic ellipsometer is also available. All the device characterization equipments are available specially suited for SiC, such as Sony/Tektronix 370A curve tracer, a HP 4155 parametric analyzer, a 500MHz digitizing scope, a computer controlled C-V and I-V measurement set up, a high temperature (up to 400°C) manual probe chuck and controller.

RPI has all the design and simulation tools that are needed for device modeling and mask layout. These include 2- and 3-dimensional numerical device and process simulators, running in a cluster of IBM RS-6000 work stations specially dedicated to semiconductor device and IC design.



(a)



(b)

Figure A-4. In operation are (a) the vertical SiC epitaxial reactor, and (b) the horizontal SiC epitaxial reactor.

CPES Key Faculty

Dushan Boroyevich

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Dr. Boroyevich is a professor of Electrical and Computer Engineering at Virginia Tech and Co-Director of CPES. He specializes in power electronics system modeling and simulation, three-phase power conversion, motor drives, and digital processor control. He earned a Ph.D. from Virginia Tech in 1986.

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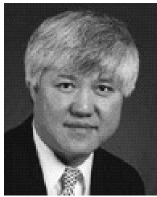

Paul Chow is a professor of electrical, computer, and systems engineering at Rensselaer Polytechnic Institute. His research interests include semiconductor devices and processes. Dr. Chow spent 12 years in industry before joining the RPI faculty. He holds a B.A. in Mathematics and Physics, and an M.S. in Materials Science. He earned a Ph.D. in electrical engineering from RPI in 1982.

Abdollah Homaifar

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Dr. Homaifar, an associate professor at North Carolina A&T, serves as director of the Autonomous Control Engineering Center. The Center is investigating the application of neural networks and fuzzy logic-based intelligent control methodologies for power electronics control. Homaifar is also coordinator of the NASA Center of Research Excellence in Aerospace. He has earned several outstanding researcher awards. He received his Ph.D. from the University of Alabama in 1986.

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Dr. Jahns is an associate director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) and a W.W. Grainger Professor of Power Electronics and Electrical Machines at the University of Wisconsin-Madison. His research interests include electric machines and actuators, adjustable-speed drives, brushless motor drives and generators, and automotive and aerospace electric systems. He earned a Ph.D. in 1978 from MIT and worked 15 years in industry before joining the faculty in 1998.

Fred C. Lee

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Fred C. Lee is a University Distinguished Professor at Virginia Tech and the founder and director of CPES. Dr. Lee has supervised to completion more than 70 masters-level and 55 Ph.D. students. He holds 35 U.S. patents and has published more than 180 journal articles and 480 technical papers. He is a Fellow of the IEEE and a past president of the IEEE Power Electronics Society. He earned a Ph.D. from Duke University in 1974. He has received multiple honorary professorships and numerous research and achievement awards, including the 1989 William E. Newel Power Electronics Award, 1990 PCIM Award for Leadership in Power Electronics Education, 1998 Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronics Systems, 2000 IEEE Third Millennium Medal, and the 2005 Ernst-Blickle Award for achievement in the field of power electronics.

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Dr. Lipo is the founder and director of the Wisconsin Power Electronics Research Center (WisPERC) and the founder and co-director of the Wisconsin Electric Machine and Power Electronics Consortium (WEMPEC). Lipo holds a W.W. Grainger Professorship in the Department of Electrical and Computer Engineering at the University of Wisconsin – Madison, and is recognized as a world authority in the design and analysis of electric machines and power electronics drives. He earned a Ph.D. in 1968 from the University of Wisconsin – Madison and worked 13 years in industry before starting his academic career. He has received several prestigious awards including being selected a Fellow of the Royal Academy of Engineering (U.K.) in 2002.

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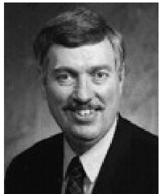

Dr. Lorenz is co-director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). He is a professor of both mechanical engineering and electrical and computer engineering at the University of Wisconsin-Madison. His research focuses on advancing the practical use of modern electronics in industrial, automotive, aerospace, and office automation systems. He earned a Ph.D. from the University of Wisconsin-Madison and worked 12 years in industry prior to joining the faculty in 1984.

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G.Q. Lu received a double-major B.S. degree in Physics and Materials Science and Engineering from Carnegie-Mellon University in 1984. He then went on to Harvard University, where he earned M.S. and Ph.D. in Applied Physics by 1990. Immediately afterwards, he worked as a staff engineer at ALCOA Electronic Packaging, Inc. for two years.

Dr. Lu became faculty at Virginia Tech in 1992, as an Assistant Professor in the Department of Materials Science and Engineering. Since 2003, he has been Professor in both departments of MSE and Electrical and Computer Engineering.

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Khai Ngo received a B.S.E.E. from California State Polytechnic University in 1979, and M.S. and Ph.D. degrees in Electrical Engineering from California Institute of Technology in 1980 and 1984, respectively. From 1984 to 1988, Dr. Ngo worked at General Electric Corporate R&D. Khai then joined the University of Florida in 1988, and has been a professor in their Department of Electrical and Computer Engineering since.

Dr. Ngo's research interests include, among others, magnetic materials, power electronic circuits and control, power semiconductor devices and integrated circuits, elevated-temperature design, and RF power electronics.

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Elaine Scott received B.S. and M.S. degrees in Agricultural Engineering from the University of California–Davis in 1979 and 1981, respectively. Elaine then received a Ph.D. in Agricultural Engineering in 1987, and a Ph.D. in Mechanical Engineering in 1990, both from Michigan State University.

Dr. Scott served as assistant professor in the Department of Mechanical Engineering at Michigan State University from 1990-1992. She has been a professor in Virginia Tech's Department of Mechanical Engineering since 1992. In 2003, Elaine became the Acting Director of the Virginia Tech – Wake Forest University School of Biomedical Engineering and Sciences.

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Jacobus Daniel van Wyk received the M.Sc.Eng. degree from the University of Pretoria, Pretoria, South Africa, in 1966, the Dr.Sc.Tech. degree from the Technical University of Eindhoven, Eindhoven, The Netherlands, in 1969, and the D.Sc. degree (with high honors) in engineering from the University of Natal, Natal, South Africa, in 1996.

He has worked with the S.A. Iron and Steel Corporation, the University of Pretoria, and was a member of the Technical and Scientific Staff, University of Eindhoven, from 1961 to 1971. From 1971 to 1995, he was a Chaired Professor of electrical and electronic engineering at the Rand Afrikaans University, Johannesburg, South Africa, holding Chairs in electronics and in power electronics until 1992. He founded the Industrial Electronics Technology Research Group, Faculty of Engineering, in 1978 and directed this unit until 1999. Since July 1995, he has held a special University Council Research Chair in industrial electronics at the Rand Afrikaans University. He joined The Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, in January 2000, where he is the J. Byron Maupin Professor of Engineering, working in the National Science Foundation Engineering Research Center for Power Electronics Systems.

Dr. van Wyk received 20 prize paper awards including 11 IEEE prize paper awards, the prestigious IEEE William E. Newell Power Electronics Award in 1995, an IEEE Third Millennium Medal in 2000, and a range of other awards from IEEE Societies as well as from the South African Institute of Electrical Engineers. He is a Fellow of the South African Institute of Electrical Engineers. He is active in several capacities within the IEEE and its Societies.

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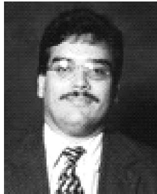

Miguel Velez is a professor of electrical and computer engineering at the University of Puerto Rico – Mayagüez. He is the recipient of the Presidential Early Career Award for Scientists and Engineers, the highest honor bestowed by the U.S. government on scientists and engineers at the outset of their independent research careers. He also was honored as a UPRM CEC Distinguished Professor and a Distinguished Engineering Faculty member by the Puerto Rican Professional Engineering Association, Mayagüez Chapter in 1998. Dr. Velez' research interests include physical model-based signal processing and control systems with applications in electric drives and power systems. He received a Ph.D. in electrical engineering from MIT in 1992.

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Fred Wang received a B.S.E.E. from Xi'an Jiaotong University, Shaanxi, China in 1982. In 1985 and 1990, respectively, he received M.S. and Ph.D. degrees in Electrical Engineering from the University of Southern California. Dr. Wang's industry experience includes serving as Application Engineer at GE Power Systems Engineering in Schenectady, New York from 1992-1994, Senior Development Engineer at GE Drive Systems, Salem, VA from 1994-2000, and Manager at Electrical Systems & Technologies Program, GE Corporate R&D.

Dr. Wang became a Research Associate Professor at Virginia Tech in 2001, and became an Associate Professor in 2004. He has served as the CPES Technical Director since 2003. His interests are in power electronics, controls, electric machines and power systems, and motor drives.