Design Challenges of the 22 kV Solid-state Switch for Capacitor Discharge Application Based on 3.3 kV SiC MOSFET Super-Cascode

In recent years, there has been increasing demand for medium voltage (MV) power converters, driven by the necessity to enhance grid connectivity and transmission systems in light of escalating

load requirements within the grid system. Simultaneously, multilevel converters have gained significant attention due to their ability to provide efficient conversion solutions. Within the realm of MV systems characterized by elevated operating voltages, the design of auxiliary components, particularly the discharge circuit, pose formidable challenges.

The discharge circuit is crucial in MV multilevel converters, ensuring safety by dissipating stored capacitor energy during shutdown and faults. To achieve a fast discharge time and minimize losses, the external discharge method is selected by using an additional MV switch and discharge resistors. Addressing challenges related to MV levels, size constraints, and control complexity, the super-cascode topology shown in Fig. 1 is chosen as the MV switch. This design minimizes the requirements for the amount of gate drivers and power supplies, resulting in a compact design for the MV switching unit within the discharge circuit.

In the development of a 22 kV super-cascode switch designed for capacitor discharge circuit applications, 10 3.3 kV SiC MOSFETs are utilized. However, given the significant number of devices connected in series and the high operating voltage level, various issues arise, including gate oscillation and discharge. To address these challenges, circuit modifications are implemented, incorporating additional capacitor snubbers between the drain-source terminals of each MOSFET. The finalized 22 kV discharge circuit is then implemented in hardware and validated

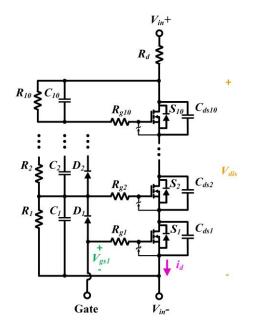


Fig.1. Schematics of the discharge circuit using the super-cascode topology as the MV switch

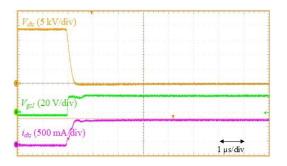


Fig. 2. The turn-on waveform of the 22 kV super-cascode switch

through experimentation. Fig. 2 illustrates the waveform of the super-cascode switch during the turn-on transient, revealing a clean and smooth device switching voltage with no observable gate oscillation or discharge issues.