3.3 kV SiC Packages with a Coaxial Commutation Loop and Uniform Interpackage Electric Field Distribution

An architecture for MV SiC packages is presented with features that aim to address known critical challenges. The proposed architecture is composed of two single switch packages as seen in Fig. 1. Key features include axial symmetry, coaxial nesting, and unique components. 3.3 kV SiC MOSFETs are used here, but many features of the architecture could be transferred effectively to other devices.

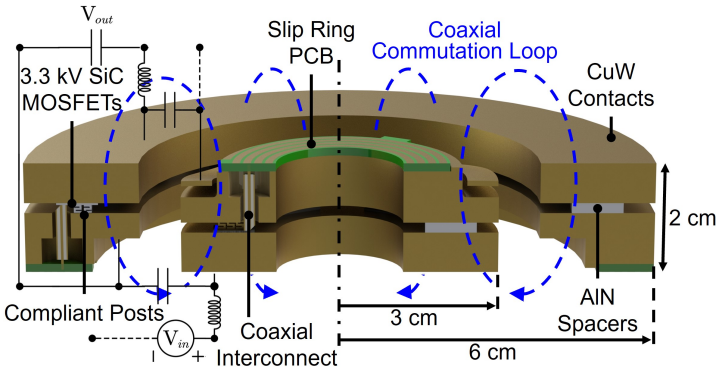

Fig.1. Cross sectional view of the coaxially nested 3.3 kV SiC packages with circuit schematic overlaid and coaxial commutation loop indicated.

The axially symmetric distributions of the components in these packages provide several benefits. One such benefit is equivalent electrical parasitics among parallel die which aids in current sharing, particularly during fast switching transients. Axial symmetry also allows for uniform temperature distributions. Using a three-die version of the inner package as an example, Fig. 2 demonstrates the equivalent peak temperatures and uniform temperature distributions among parallel die. The good current sharing and uniform temperature distributions offered by these packages means that each parallel die is electrically and thermally stressed uniformly.

The coaxial nesting and round form-factor of the packages also has some advantages. One such benefit, the coaxial commutation loop, is depicted in Fig. 1. The coaxial commutation loop provides excellent mutual inductance cancellation which helps reduce the effective power loop inductance. The Ansys Q3D-simulated power loop inductance contribution of the packages is just 2.4 nH. The other benefit of coaxially nesting packages with a round form factor is the uniform electric field between the packages. If the system input voltage needs to be adjusted, only a simple change to the radial distance between the two packages is required.

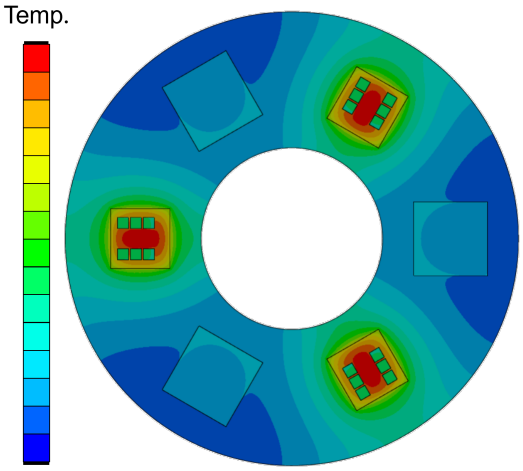

Fig. 2. Contour plot of the axially symmetric temperature distribution offered by the packages.

These packages also contain some unique components that offer their own benefits independent of the coaxially-nested structure. A combination of compliant posts and AlN spacers limit the maximum amount of mechanical stress transferred to the die and provide double-sided cooling. The coaxial gate/Kelvin interconnects limit gate loop inductance to 3 nH over the 1.5 cm distance between the die and slip ring PCB. The slip ring PCBs provide an axially symmetric interface between the packages and their gate drive circuitry.