Extraction of Common Mode Parasitic Capacitance in Balance Filter for The Prediction of EMI Noise Suppression

Fig.1 shows the 1kW single-phase totem-pole PFC converter in which balance technique is applied. Fig.2 shows the CM noise equivalent circuit. A is the switching node of the converter. B is the input AC or DC voltage source. C is the PCB ground of the converter. D is the earth ground which is usually connected to the grid earth. Except for the coupled inductor half bridge, the parasitic capacitance C2 and C3 in Fig. 2(a) form the other half bridge. C2 is the parasitic capacitance of the converter switching node referring to the earth ground. C3 is the capacitance of the converter PCB ground referring to the earth ground. To block the CM noise, the following equation should be satisfied throughout 150kHz to 30MHz to maintain equal voltage potential at point B and D by adding an extra small capacitor Cadd in parallel with C2 or C3, as Fig.2(b) shows.

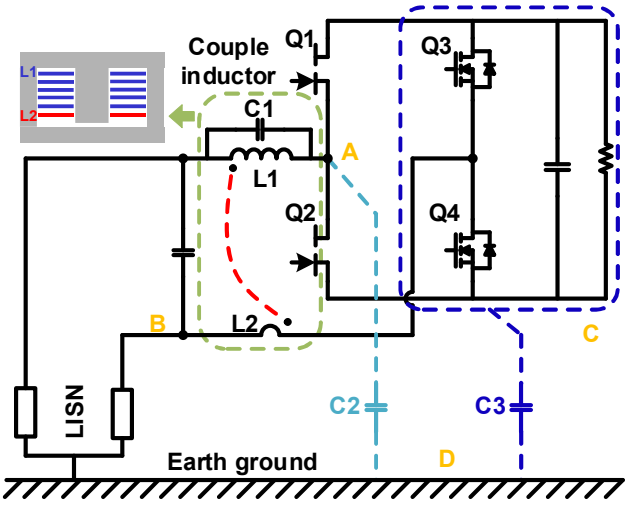

Figure 1: Balance technique applied in Totem-Pole PFC

$$\frac{V_{AB}}{V_{BC}} = \frac{V_{AD}}{V_{DC}} \qquad (1)$$

The concept of the balance is simple since it's a Wheatstone bridge. The difficulty is to extract the parameters in the bridge and predict the noise attenuation with the parameters. The exact value of C2 and C3 is essential to the selection of Cadd. Impedance analyzer is most commonly used for parasitic capacitance extraction. However, the self-parasitic parameters of the impedance analyzer probe introduce extra resonance and severely impact the accuracy of these PCB capacitance.

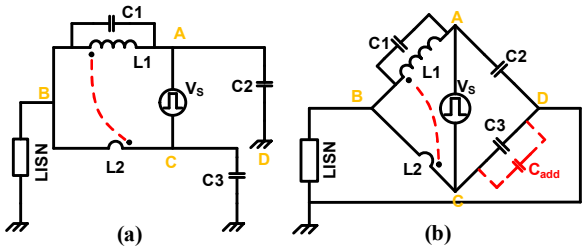

Figure 2: Simplified balance network

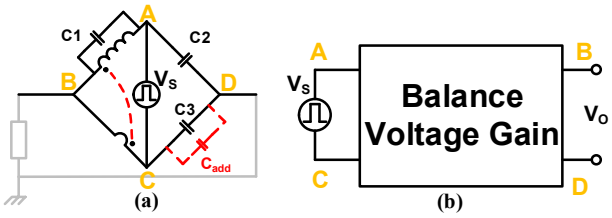

Figure 3: Balance filter model

On the other hand, the balance network is intrinsically a filter even without adding any capacitor to make the bridge balanced. Theoretically, the noise from the source could be totally attenuated if (1) were maintained. Therefore, the prediction of the noise attenuation in balance network is important to meet the EMI standard and simplify the input filter design. Considering balance network in Fig.3(a) as a filter, then the noise current flowing through the LISN is the load. The insertion voltage gain of the balance filter in Fig.3(b) can be identified if all the parameters are correctly extracted. In the other word, balance filter can be used to verify the correctness of the parameters. In Fig.3, A-C is the noise input which is the switching transition of the main devices and B-D is output. Disconnecting the 50Ω LISN network, B-D will have a very high impedance and can be considered as open circuit. In this way, the modeling of the balance filter will be greatly simplified.