Wide Bandgap High Power Converters & Systems (WBG-HPCS) Consortium Nuggets

Figures-of-Merit and a Current Metric for the Comparison of IGCTs and IGBTs in Modular Multilevel Converters

IGCTs and IGBTs are compared in the case of a HVDC MMC. Because of the different principles IGBTs and IGCTs operate on, they cannot be compared directly from the figures quoted in their datasheets. Therefore, we introduce new figures of merit (FOMs) and a current metric, as a means for easy and accurate selection of semiconductor switches for an MMC application. Simulation is used to validate the FOMs. This analysis supports the growing interest in IGCTs for MMCs that can be seen in some papers.

Using an analytical model of the MMC, an equivalent current rating to the IGBT dc-current has been built for the IGCT based on the IGCT average current. The ratings of the different semiconductors are displayed Fig. 1.

Two figures of merit have been built to reflect the losses of the semiconductors: the conductive losses for one FOM, and the switching losses for the other one. The conductive losses' FOM is the ratio between the average on-state voltage and the blocking voltage. The switching losses' FOM is the ratio of the switching energy (written on the datasheet) over the product of the current and the voltage used for the measure of the datasheet switching energy.

To verify the relevance of those FOMs, the losses of the semiconductors have been calculated with an MMC dynamic model, imitating a real-time MMC operation, with a balancing control algorithm and a nearest level modulation MMC control. For the particular case of one MMC, Fig. 2. illustrates the coherence between the FOMs (left) and the simulated losses (right).

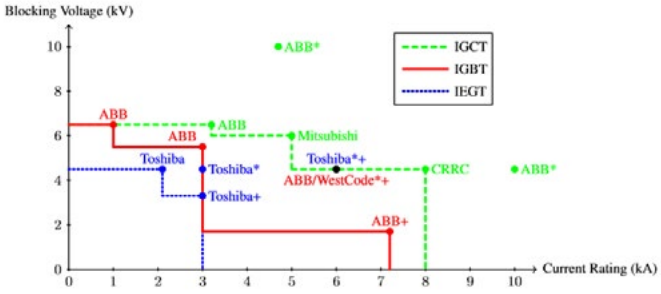


Fig. 1. Ratings of semiconductors with the current rating of the paper.

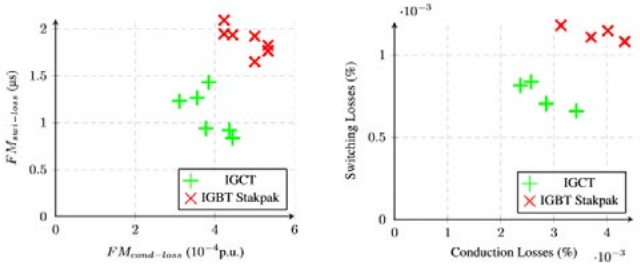


Fig. 2. Comparison of the losses in MMC (right) and the FOMs developed in the paper (left).

Characterization, Reliability and Packaging for a 300° C SiC MOSFET

This paper presents work done to explore the temperature limits of current generation SiC MOSFETs and provides the groundwork for developing a power module capable of reliable operation at ambient temperatures of 250° C. Since device self-heating causes the junction temperatures to be greater than 250° C, testing was performed at 300° C.

A three-terminal package is developed for high-temperature testing. Static characterization is performed for the custom package. Finally, reliability tests in the form of high temperature gate bias (HTGB) and high temperature reverse bias (HTRB) conditions are performed to determine the elevated temperature lifetime of SiC MOSFETs.

Fig. 1 shows the high temperature package created for reliability testing. A 1 kV SiC Wolfspeed CPM3-1000-0065B MOSFET die is selected for testing.

Fig. 2 shows the results for the HTGB and HTRB tests. These tests were designed in accordance to standards listed in JEDEC's A108C and Automotive Electronics Council's (AEC) Q101 forms. Incremental static characterization was performed on the devices during the test. Every 100 hours, the devices were measured on the Agilent B1505A curve tracer. Failure was defined to be any characteristic outside of nominal datasheet values.

Although successful static characterization at 300° C supports the idea that short-term operation of SiC MOSFETs at high temperatures is possible, experimental results show that current generation SiC MOSFETs are not reliable at temperatures of 300° C. The devices quickly break down over a period of 300 hours when stressed with accelerated lifetime bias tests.

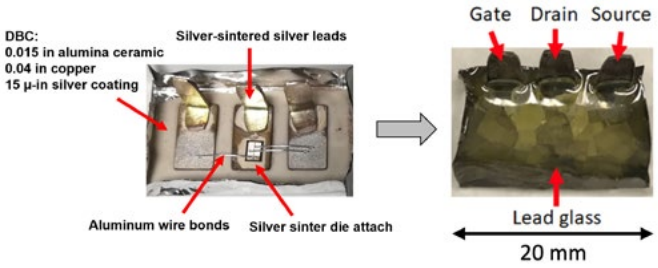


Fig. 1. High temperature package for SiC MOSFET.

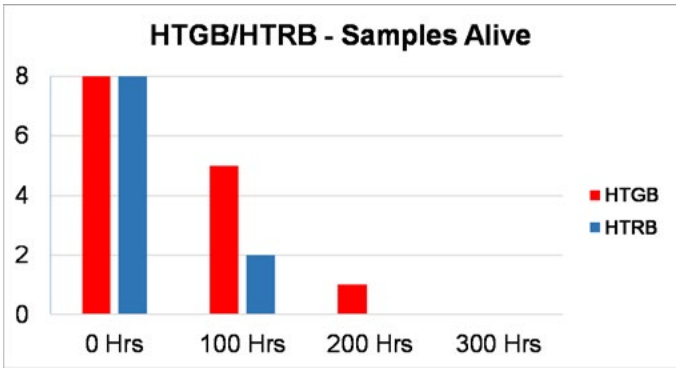


Fig. 2. Failure rate of HTGB and HTRB tests.

Imbalance Mechanism and Balancing Control of DC Voltages in a Transformerless Series Injector Based on Paralleled H-Bridge Converters for AC Impedance Measurement

Small-signal stability of ac power systems can be assessed by measuring terminal impedances with a transformerless series injector for wideband measurement of source and load impedances. A typical implementation of the transformerless series injector is a paralleled H-bridge (PHB) converter, shown in Fig. 1, where dc voltage imbalance will occur when the system-current magnitude is larger than a critical threshold, and thus the operation region of the series injector is seriously restricted. To address this issue, this work presents a deep analysis of the mechanism behind dc voltage imbalance for a PHB-based series injector, and reveals that positive feedback exists in the dc voltage-balancing loop under high system-current magnitude. An enhanced control scheme is proposed to balance dc voltages in the full system-current range, where a reactive component is injected in the output voltage while a reactive circulating current is introduced among H-bridge converters for redistributing active power. The imbalance mechanism of dc voltages in the existing control scheme is analyzed, revealing that positive feedback appears in the dc voltage balancing loop when the system-current magnitude exceeds a critical threshold determined by the power losses characteristic of H-bridge converters. Furthermore, an enhanced control scheme is proposed to make the PHB operate safely in the full system-current range by introducing reactive components in output voltage and a reactive circulating current among H-bridge converters for redistributing active power. The proposed scheme also proves that dc voltages of PHB can be balanced within the full system-current range with a properly designed reactive component magnitude of the output voltage. The imbalance mechanism of dc voltages in the existing scheme and the feasibility of the proposed scheme are demonstrated by both simulation and experimental results. The proposed control scheme extends the system-current capability of PHB and will be attractive in ac impedance measurement applications.

The system behavior with the proposed scheme is comprehensively analyzed in this paper, and the reference design for the injected reactive component magnitude in the output voltage is offered. Finally, the imbalance mechanism and the proposed scheme are validated by simulation and experimental results.

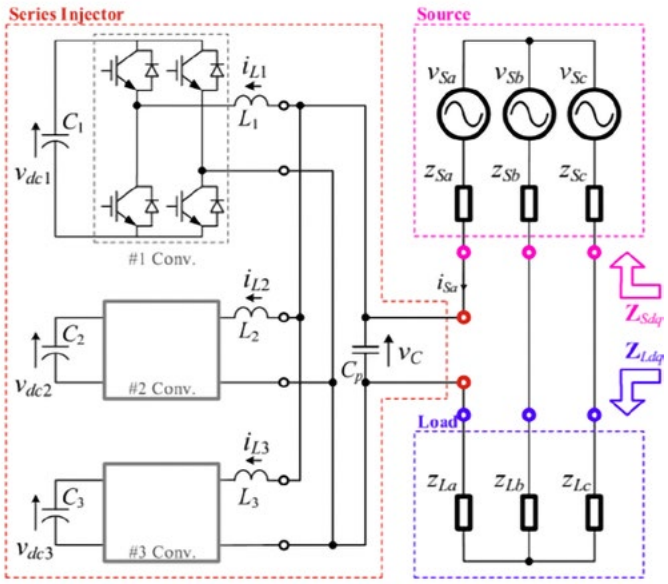


Fig. 1. Power stage of the impedance measurement setup for a three-phase ac power system using a transformerless series injector based on three PHB converters.

Three-Terminal Common-Mode EMI Model for EMI Generation, Propagation, and Mitigation in a Full-SiC Three-Phase UPS Module

With superior loss characteristics, wide bandgap devices such as silicon carbide (SiC) MOSFETs are expected to replace Si-IGBTs in grid-connected applications. Uninterruptible power supply (UPS) is an application in which low loss from SiC devices can largely improve the system efficiency. However, fast switching of a SiC MOSFET worsens the electromagnetic interference (EMI). In addition, the UPS is comprised of multiple converters wherein different combinations of the converters take part in power transfer depending on the mode of operation. This complicates the prediction and strategies for noise, especially the common-mode (CM) part.

The UPS under study is composed of three power conversion stages: a rectifier, an inverter for ac-ac conversion, and an active battery charger with a battery rack as energy storage. The complete UPS model for EMI is derived as shown in Fig. 1. The common-mode voltage (CMV) of each power conversion stage ($v_{cm,REC}$, $v_{cm,INV}$, $v_{cm,DCDC}$) is defined as the average terminal output voltage referring to the mid-point of the dc-link. The model also includes the impedance of the LISN (Z_{LISN}), the impedance of the resistive loads (R_{LOAD}), the impedance of the switching harmonic filters ($Z_{f,ac}$, $A_{f,dc}$), as well as the parasitic components (C_s, C_{s2}, C_{bus}, $C_{cabinet}$, and $L_{cabinet}$).

The model provides insight into how CM noise will change when the dc-dc converter operates. When it operates, the CM noise generated by the rectifier, inverter, and dc-dc converter propagates through the battery cabinet to the ground. Within this path, the parasitic components of the battery cabinet are present and create resonances with the dc inductor. Together with additional CMV generation, these resonances deteriorate the CM noise profile.

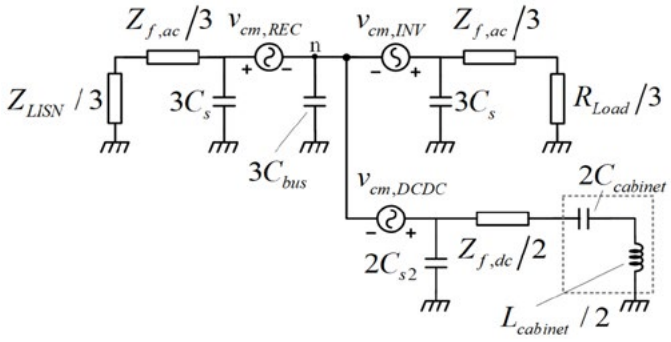


Fig. 1. CM EMI model of UPS and noise propagation paths to LISN.

Based on the developed model, an EMI mitigation strategy for UPS is investigated with the focus on topology and PWM scheme selection. The three-level topology with LMZVM is selected for the rectifier and inverter implementation as it has lower CM emission and provides a good control of neutral point voltage. The three-level bi-directional dc-dc converter with a synchronized switching sequence is selected for the dc-dc stage as it has eliminated CM emission in ideal conditions, and it provides good manufacturability by sharing the same phase-leg with the ac-ac stage.

A 20 kW full SiC UPS has been built to verify the impact of dc-dc converter operation and the mitigation strategy. All the power conversion stages utilize 1.2 kV 40 A full-SiC NPC modules and have a switching frequency of 60 kHz. The CM noise spectra for two different modes of operation are compared, as shown in Fig. 2. With the dc-dc converter operation, the CM harmonic component at 180 kHz is increased by 6.8 dB. This is critical for the EMI filter design. Over 1–2 MHz, the CM noise has been increased by a maximum of 12.5 dB. Over 2–30 MHz, a high increase in the CM noise was observed, which does not exist in the double-conversion mode.

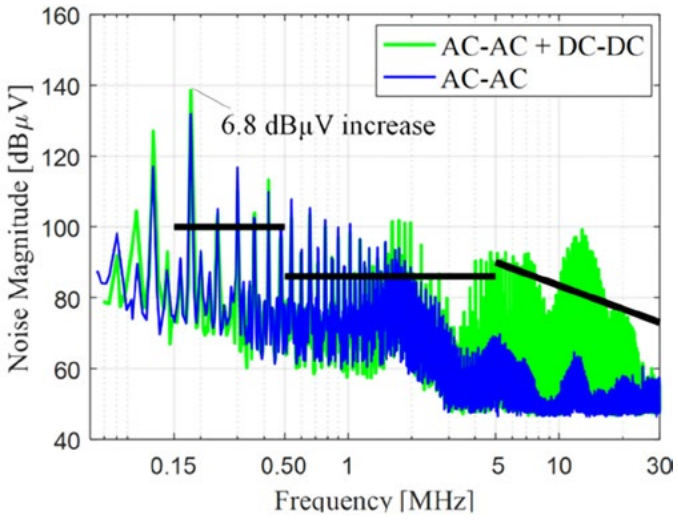


Fig. 2. Experimental results for CM EMI depending on the modes of operation.

A Series-Series-CL Resonant Converter for Wireless Power Transfer in an Auxiliary Power Network

This paper proposes a 1 MHz switching frequency, 48 V to 48 V, 92%-efficiency series/series-CL (S/S-CL) GaN-based resonant converter for wireless power transfer. This type of topology can compensate reactive power, thus increasing system efficiency, generating a constant output voltage that can be tuned by changing one pair of LC parameters, and keeping a symmetrical coil structure, simplifying design and optimization.

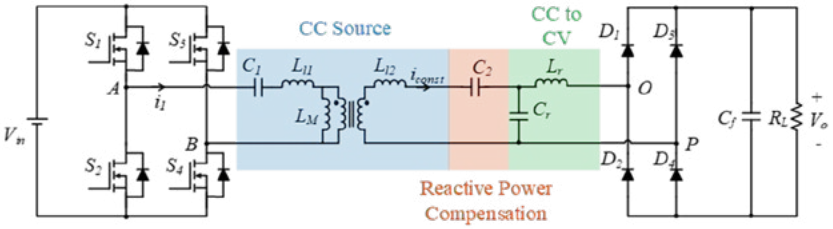
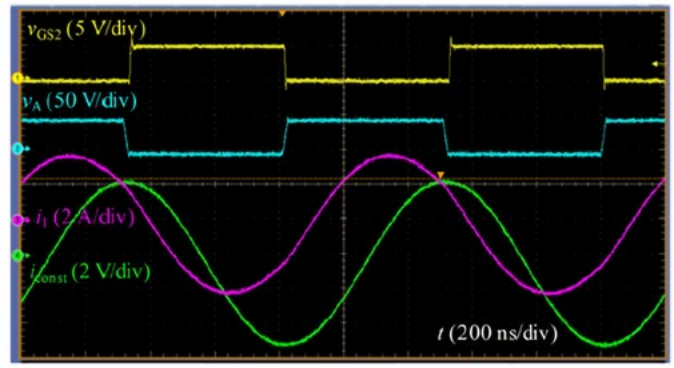


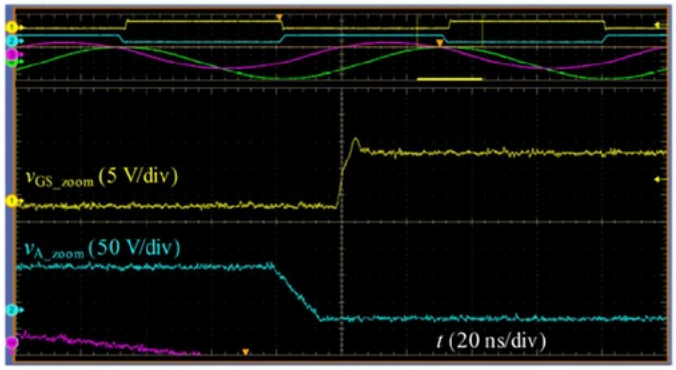
Fig. 1. S/S-CL topology for wireless power transfer converter.

As shown in Fig. 1, an S/S-CL topology is proposed to meet all the requirements for the WPT as the auxiliary power supply. Capacitor C_1 is in resonance with the self-inductance of the primary side coil L_{l1} working as a constant current source. The capacitor C_2 is used to adjust the load impedance of the full-bridge inverter to reduce reactive power and achieve ZVS for primary-side MOSFETs. The C_rL_r pair will change the constant current (CC) source to a constant voltage (CV) source, forming a load-independant voltage source. This topology can thereby achieve coupling-independent resonant frequecy and load-independent output voltage, and the output voltage can be adjusted by changing a pair of LC parameters.

Fig. 2 shows the gate signal, jumping node voltage, and current of both the primary and secondary side. From the zoomed-in waveform, ZVS is achieved for soft switching, and i_1 is almost in-phase with v_A, which means the system reactive power is minimized.



(a) v_{GS2}, v_A, i_1, and i_{const} waveform of WPT $C_2 = 2.547$ nF.



(b) Zoomed-in waveform showing the ZVS of the WPT $C_2 = 2.547$ nF

Fig. 2. Operating waveforms of the WPT converter.

Development of an Impedance Measurement Unit for 1 kV DC and 800 V AC Systems

The small-signal instability of ac-dc power systems with multiple power electronics converters interconnected can be effectively analyzed by applying a Nyquist criterion to their small signal terminal impedances. The impedance measurement unit (IMU) is a professional setup used to characterize the terminal impedance of both the source subsystem and the load subsystem. The IMU injects a small perturbation signal at various selected frequencies into the system, while corresponding responses of current and voltage at the subsystem terminals are recorded and then processed to compute subsystem impedances over the frequency range of interest.

Fig. 1 shows the IMU power-stage topology capable of characterizing impedances of 1 kV dc and 800 V ac networks in the frequency range of 10 Hz–1 kHz. The power-stage comprises three power electronics building blocks (PEBBs) and a switching network. Each PEBB is an H-bridge converter with maximum 200 A current capability and 1 kV-rated dc-side voltage and is built using 1.7-kV SiC MOSFET. By configuring the state of the switching network, the IMU can work in shunt current and series voltage injection mode, both of which are needed to accurately measure subsystem impedances. In shunt mode, PEBBs are configured as a five-level cascaded H-bridge converter with 3 kV dc voltage in total to inject current perturbation for source impedance characterization. In series mode, PEBBs are configured as a parallel-interleaved converter to inject voltage perturbation for load impedance characterization, and controlled to equally share the system current. The IMU control is implemented based on the distributed control scheme in which PWM signals of each PEBB are generated by a local slave controller, and a master controller connects with all slave controllers through a ring-type communication network to obtain circuit states and realize high-level control. The IMU is designed and implemented with a modular and scalable structure and consequently can be extended to medium voltage level.

A hardware prototype has been bulit as shown in Fig. 2 and tested at the rated working condition to validate its impedance iditification capability.

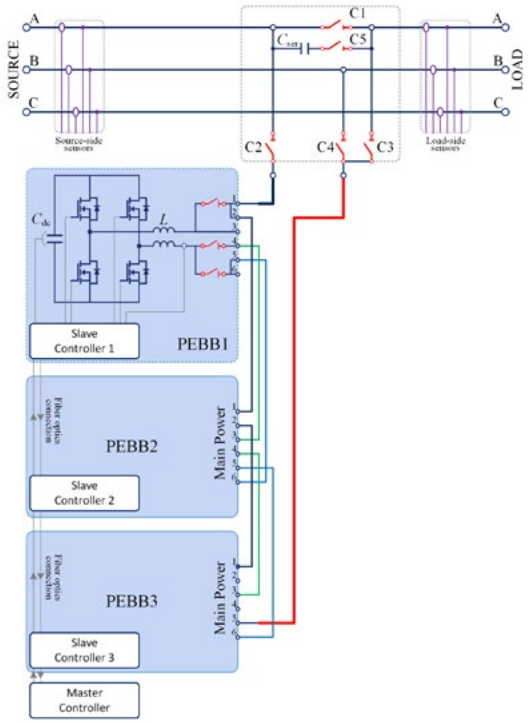


Fig. 1. Power stage of the impedance measurement setup.

Fig. 2. IMU hardware prototype.

Design and Assessment of a Medium-Voltage Power Cell Based on High-Current, 10 kV SiC MOSFET Half-Bridge Modules

Rapid technology improvement of SiC MOSFET transistors combined with their extraordinary characteristics are key drivers for their utilization in medium-voltage (MV) applications. For typical MV modular converter applications, the power cell is a critical piece. Power cell systematic design and assessment methodology are crucial for preventing damage and for full testing that also explores capabilities prior to implementation at the converter level. Proven successful utilization of SiC MOSFET devices, together with their superior characteristics, are slowly overtaking power cell designs, currently dominated by Si IGBTs. Recent advances have been made in the design of power cells with 1.2 kV, 1.7 kV and 10 kV SiC MOSFETs.

Accordingly, design considerations and available solutions for the design of a power cell utilizing high current, 10 kV, SiC MOSFETs in MV applications is presented. Furthermore, the systematic design and assessment framework process of the power cell is provided. Critical insulation considerations and testing procedures are described, confirming partial-discharge-free (PD-free) operation at the rated voltage of the power cell. Safe operating area (SOA) is derived for a single dc-dc case with a duty cycle of 50% for a designed cooling system. However, the described methodology would be the same for any case in dc-dc or dc-ac operation mode. The thermal model is 90% accurate, showing an acceptable maximum difference of 8° C, which is, considering the complexity of the system and its cooling, extremely valuable for proving thermal modeling methodology. Additionally, the designed enhanced gate-driver (eGD) successfully deals with electromagnetic interference (EMI) issues caused by having high slew rate voltage transients. The designed MV power cell (shown in Fig. 1) for utilization in modular multilevel converter (MMC) applications having the latest 10 kV SiC MOSFET half-bridge (HB) module achieved power density (PD) ≥ 10 kW/l, η ≥ 99% (shown in Fig. 2) and successfully operated at V_{dc} = 6 kV, I = 84 A, f_{sw} ≥ 5 kHz, Tj ≤ 150° C in both both dc-dc and dc-ac mode, having high-switching speeds up to dv/dt ≈ 100 V/ns.

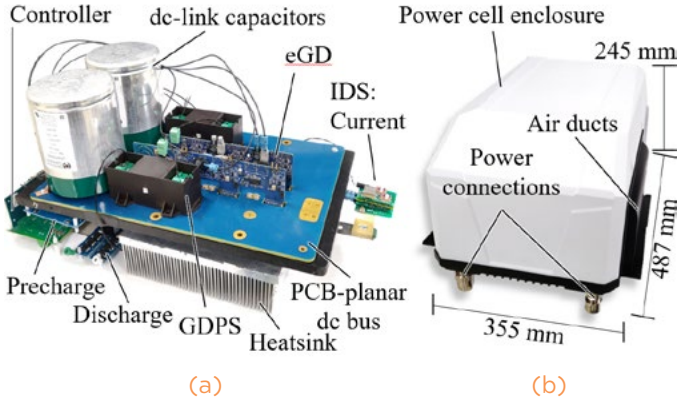


Fig. 1. Photographs of the 10 kV SiC MOSFET-based half-bridge power cell (a) power cell with constitutive parts outside enclosure, (b) power cell enclosure. Power density: 11.9 kW/L (195 W/in³), calculated based on maximum input values. All clearance and creepage distances and solid insulation material thicknesses comply with the IEC 60664.

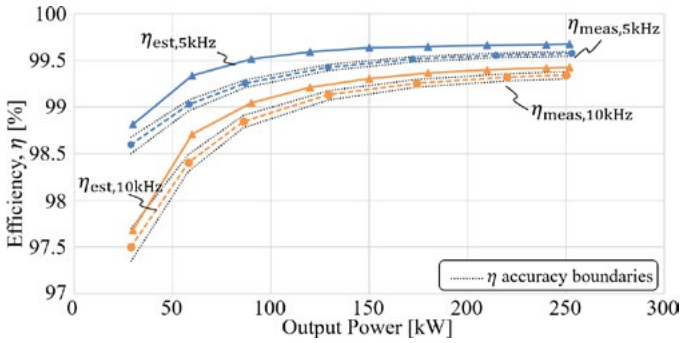


Fig. 2. Comparison between estimated and measured power cell efficiency for variable current range, V_{dc} = 6 kV, duty cycle d = 50% in dc-dc pumpback, at 5 kHz and 10 kHz.

Smart Nanogrid System and Energy Management Algorithm for Sustainable Houses

Technology advancements that happened in the last two decades have changed the way how people live, interact, and work more than any technology in the past 100 years. Not only little "gadgets" enabled this enormous paradigm shift; the new innovative concepts have been well integrated into the design and manufacturing of computers, appliances, automobiles, airplanes, and ships, and more recently, these concepts are being applied to the homes where building practices, by contrast, experienced a very slow, if not resistant effort to advance. Interest has grown since Virginia Tech's demonstration of the use of advanced manufacturing concepts, prefabricated structures, and a great number of power electronics to redefine the conventional practice of modern home design. Its smart house, called FutureHAUS, won first place at the international competition in Dubai, UAE, validating an enormous societal desire to see this technology implemented. CPES was a major contributor to this gratifying victory.

FutureHAUS featured a CPES-designed, advanced power electronics system—a nanogrid, built to achieve a net-positive energy balance in the FutureHAUS, utterly minimizing, if not eliminating, utility grid dependence. Fig. 2 shows the utilization of solar energy during the test period (the dashed black line shows cumulative power production, the solid one is cumulative consumption, and the red shows solar power production). It comprised five solar arrays, aggregately contributing close to 14 kW of peak power. Each solar array featured a dedicated charge controller for increased reliability, as well as for independent, per string, maximum power point tracking. An installed 14 kWh battery was the safest and least polluting rechargeable battery that could be found on the market, built with very high environmental standards and safe to be stored indoors with no need for venting or cooling. Furthermore, the efficient and contemporary 8 kW power inverter interfaced photovoltaics and batteries with the utility grid and served as a main generator of the FutureHAUS clean energy. This inverter has been controlled with an advanced energy management algorithm that goes beyond the traditional residential system control. This paper gives an overview of the whole project with a focus on the technical description of the FutureHAUS nanogrid system and energy management algorithm.

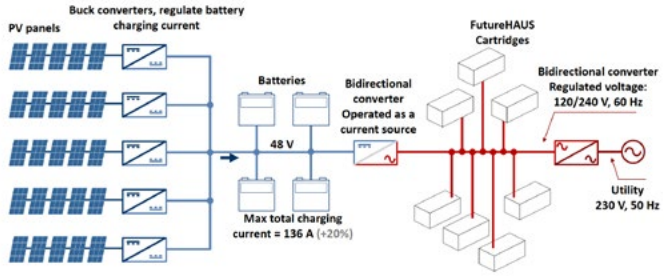


Fig. 1. FutureHAUS nanogrid system.

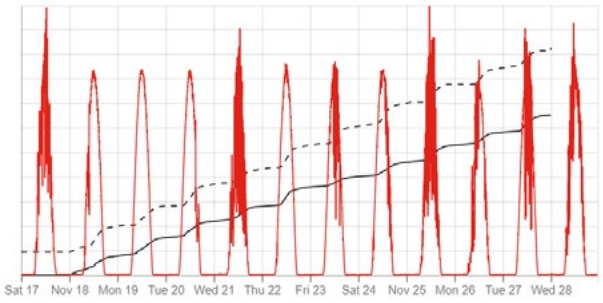


Fig. 2. Solar energy utilization.

Stability Analysis of Power Systems with Multiple STATCOMs in Close Proximity

Recently, multiple static synchronous compensator (STATCOM) units have been adopted in power transmission systems to obtain a better voltage regulation and to share loads. However, as in Fig. 1, these units and systems could possibly interact in a negative way instead of helping each other due to the improper design of the STATCOM controllers. To analyze this problem, a d–q frame impedance-based stability analysis was used to explore the instability with the presence of STATCOMs, where previous stability-related findings are not applicable directly because of some unique STATCOM features. This paper identifies the frequency range of interactions from the viewpoint of d–q frame impedances and pinpoints that the ac voltage regulation was the main reason for instability, masking the effects of a phase-locked loop (PLL) on power transmission systems. In addition, due to the high impedance of STATCOMs around the frequency range of interactions, the number of connected STATCOMs was the main contributor to instability instead of the topology of power systems or the locations of the STATCOMs. A scaled-down 2-STATCOM power grid was built to verify the conclusions experimentally. This paper is accompanied by a video showing instability between STATCOMs in the experiment.

In this work, potential instability in power systems with multiple STATCOMs in proximity was found due to the design of STATCOM controllers: the ac voltage controller, the PLL, and the QV droop controller. A d–q frame impedance-based stability analysis was used to explore the instability. From the analysis, the following conclusions were obtained. First, STATCOMs were seen to interact with each other through the transmission lines due to the relatively high magnitude of their impedances with respect to those of the lines. Second, the use of d–q frame impedances identified the frequency range of interactions. The ac voltage regulation was the main reason for instability among STATCOM controllers and masked the effects of PLL in transmission systems. This kind of instability adds new knowledge about three-phase ac systems, besides CPL dynamics and synchronization, with the presence of STATCOMs. Although STATCOMs synchronize with the power grid, the instability is nonetheless due to ac voltage regulation. Third, due to the large impedance of STATCOMs around the frequency range of interactions, the number of connected STATCOMs was the main contributor to instability instead of the topology of the power system or the locations of the STATCOMs. The high magnitude of STATCOM impedance around oscillatory frequency range makes it the dominant reason for instability, while the topology of the power systems showed negligible influences. The use of alternative controllers could improve stability conditions, as they can damp the resonant peak in the STATCOM impedance, which could cause instability. However, this cannot avoid the onset of instability. Finally, a scaled-down, two-STATCOM power grid was built to verify the conclusions experimentally. Finding parameters that help in stabilization using the impedance-based method is essential but not easy because it is hard to correlate a specific control parameter to stable regions using simplified and straightforward relationships, as the exact parameter ranges that stabilize the system vary with the system parameters, such as line impedances, load flows, etc. This will be a future path of exploration.

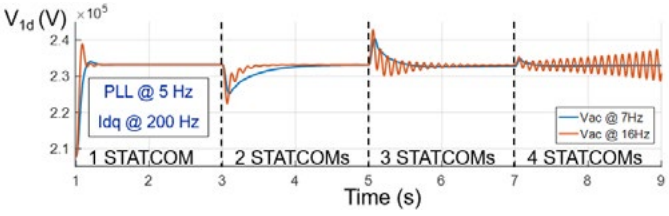


Fig. 1. Potential instability due to ac voltage loop.

Analysis of STATCOM Small-Signal Impedance in the Synchronous D-Q Frame

Small-signal model impedances of grid-tied converters have recently attracted researchers' attention and have shown great importance in stability analysis. We propose an impedance model in d-q frame for STATCOMs, including dynamics from synchronization, current loops, voltage loops and QV droop, which reveals the following significant features: 1) the impedance matrix is strongly coupled in d and q channels due to nearly zero power factor; 2) different behaviors of impedances at low frequency are due to inversed direction of reactive power; and 3) coupled small-signal propagation paths of the voltage are at the point of common coupling from synchronization and ac voltage regulation. All these characteristics make it difficult to identify instability patterns and pinpoint the main contributor to instability among control loops using existing knowledge. To better understand the frequency coupling effects of STATCOMs, the d-q frame impedance model is further transformed in its complex matrix form. An example of possible instability with STATCOMs is presented and analyzed using the proposed model. The impedance model is verified experimentally with a scaled-down STATCOM prototype.

From the model proposed, the following conclusions are extracted. First, because of the inherent operating conditions of a STATCOM, the stability assessment directly from the d-q frame impedances is very difficult—as opposed to unity power factor rectifiers and inverters, for which a multivariable stability theorem using the return-ratio matrix product of the upstream and downstream impedances at a given ac interface must be used (for example, the GNC). Second, the ac voltage loop of the STATCOM is found to be the strongest contributor to its terminal impedance and consequently to its small-signal stability conditions as shown in Fig. 1. This loop was shown to effectively mask the PLL dynamics, especially for proper system parameters of transmission grids, previously shown to be critical in grid-tied power converters. Third, and very importantly, the STATCOM impedance is shown to be able to behave both as a CPL rectifier and as a grid-tied inverter injecting power into the grid, from a dynamic standpoint, featuring a negative incremental input-impedance in its Zdd or Zqq impedance elements respectively, as a function of its reactive power injection mode (capacitive or inductive), and as a function of the relative phase between the d-q frame in question and the voltage at the PCC. These are all unique impedance characteristics that make the stability analysis in the presence of STATCOMs more involved than other unity power factor converters. Fourth, alternative control is also modeled, which revealed the impacts on impedance shaping to mitigate the new instability pattern. A 2-STATCOM study case is simulated that validated the above conclusions. Lastly, the model is verified experimentally using an IMU to measure the input-impedance of a 10-kVAR STATCOM prototype, which is shown to match up very well with the impedance obtained using the developed model.

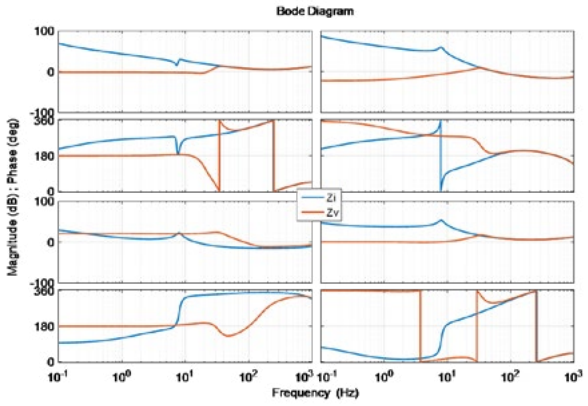


Fig. 1. STATCOM impedances: with current loop (Zi) and with all loops (Zv).

A Synchronous Distributed Control and Communication Network for SiC-Based Modular Power Converters

A communication protocol is proposed and implemented on a four-node converter shown in Fig. 1. The distributed communication system consists of one master and three slaves with linear daisy chain topology. The custom-made controller hardware is designed at CPES, based on a TI TMS320 DSP and an Altera MAX 10 FPGA. The closed-loop control algorithm is mainly implemented in the DSP, and the communication protocol is mainly implemented in the FPGA. In addition to the communication network between the master controller and the slave controllers, there is also communication inside each node. For example, in the slave node, the slave controller communicates with four gate drivers and two sensors, including one current sensor to measure the inductor current of the PEBB and one voltage sensor to measure the dc capacitor voltage of the PEBB. All of the sensing data will be transmitted to the master controller for the closed-loop control.

Since each PEBB is controlled by an individual controller, the synchronization among all of the controllers needs to be realized for the converter operation. The synchronization accuracy for four nodes is 25 ns. Based on the synchronization, the interleaved PWM waveforms for the three slaves are shown in Fig. 2. On the left is the trigger signal of a switching cycle for the three slaves, and on the right is the PWM waveform. The switching frequency for each PEBB is 20 kHz, and the communication frequency is 120 kHz.

In summary, a synchronous distributed control and communication protocol is designed and verified for a SiC-based modular power converter. A new synchronization method based on the oversampling clock and data recovery syntonization and PTP-based synchronization is implemented in the system. The synchronization can be well controlled with the maximum synchronization accuracy of 25 ns among four nodes. A control and communication frequency of 120 kHz is realized with a custom-defined packet and protocol.

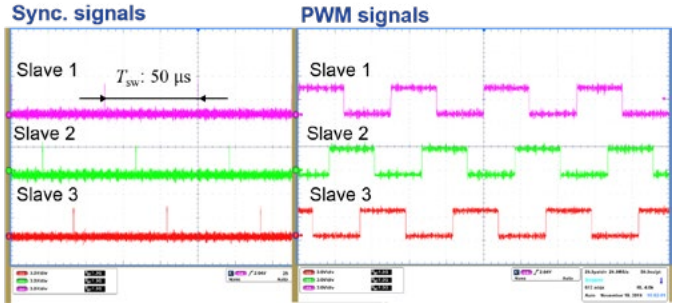


Fig. 2. Interleaved PWM generation for three slaves.

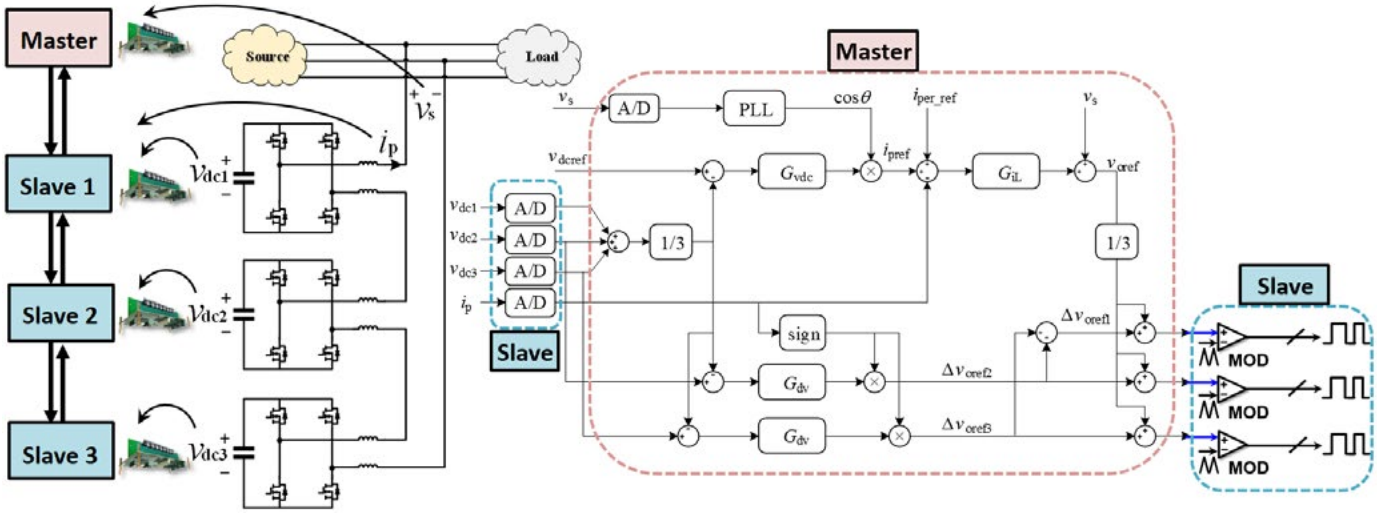


Fig. 1. Distributed control and communication network for the converter.