



US007071660B2

(12) **United States Patent**
Xu et al.

(10) **Patent No.:** **US 7,071,660 B2**
(45) **Date of Patent:** **Jul. 4, 2006**

(54) **TWO-STAGE VOLTAGE REGULATORS WITH ADJUSTABLE INTERMEDIATE BUS VOLTAGE, ADJUSTABLE SWITCHING FREQUENCY, AND ADJUSTABLE NUMBER OF ACTIVE PHASES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/018,920**

(22) Filed: **Dec. 22, 2004**

(65) **Prior Publication Data**
US 2005/0184713 A1 Aug. 25, 2005

Related U.S. Application Data
(63) Continuation-in-part of application No. 10/781,931, filed on Feb. 20, 2004.

(51) **Int. Cl.**
H02M 3/158 (2006.01)
(52) **U.S. Cl.** **323/266; 323/272; 323/284; 323/282**
(58) **Field of Classification Search** **323/266, 323/272**

See application file for complete search history.

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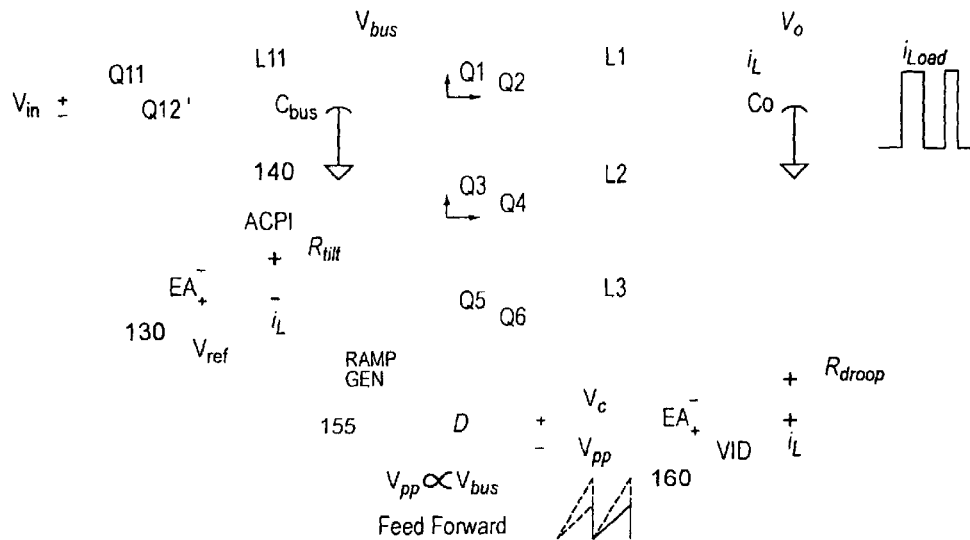
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(57) **ABSTRACT**

A two-stage power converter that dynamically adjusts to output current requirements includes a first stage regulator that provides power to a second stage regulator. The first stage can be a buck converter, and the second stage can be a multiple-phase buck converter. The output voltage of the first stage (intermediate bus voltage V_{bus}) is varied according to the load current to optimize conversion efficiency. To provide maximum efficiency, the V_{bus} voltage is increased as load current increases. The V_{bus} voltage provided by the first stage can be varied by duty cycle or operating frequency control. In another embodiment, the switching frequency of the second stage is varied as output current changes so that output current ripple is held constant. In an embodiment employing a multiple-phase buck converter in the second stage, the number of operating phases are varied as output current changes.

20 Claims, 19 Drawing Sheets



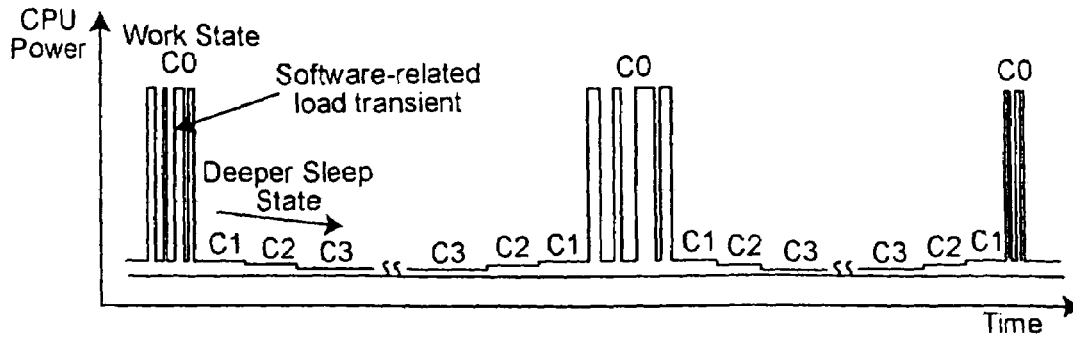


Figure 1

Measured Overall Efficiency vs. V_{bus} at Different Loads
 ($V_{in}=16V$, 1MHz, With Drive Loss)

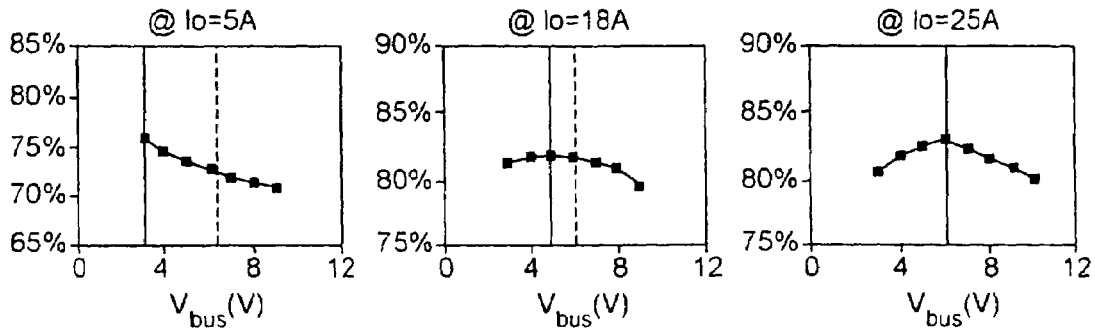


Figure 2

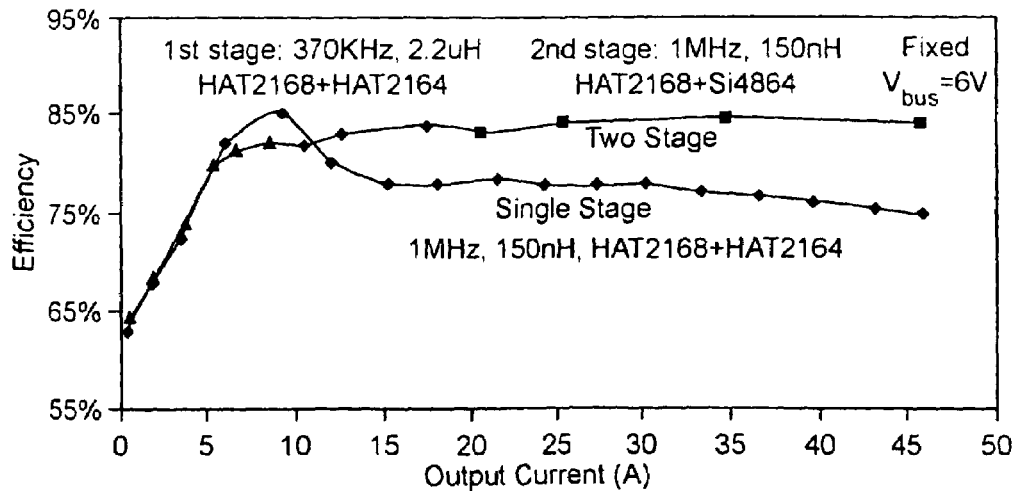


Figure 3A

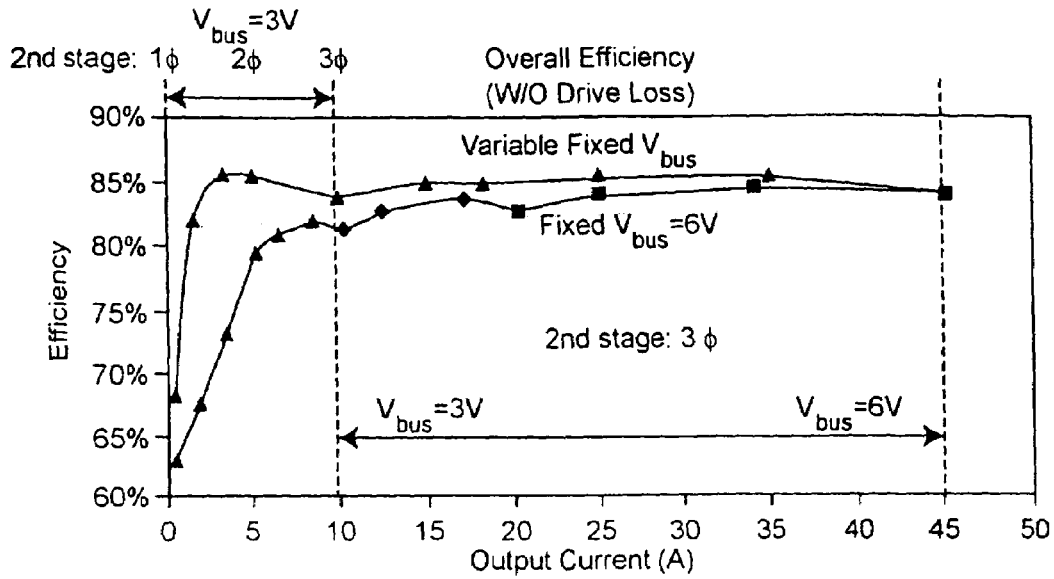


Figure 3B

Global System Power States and Transitions

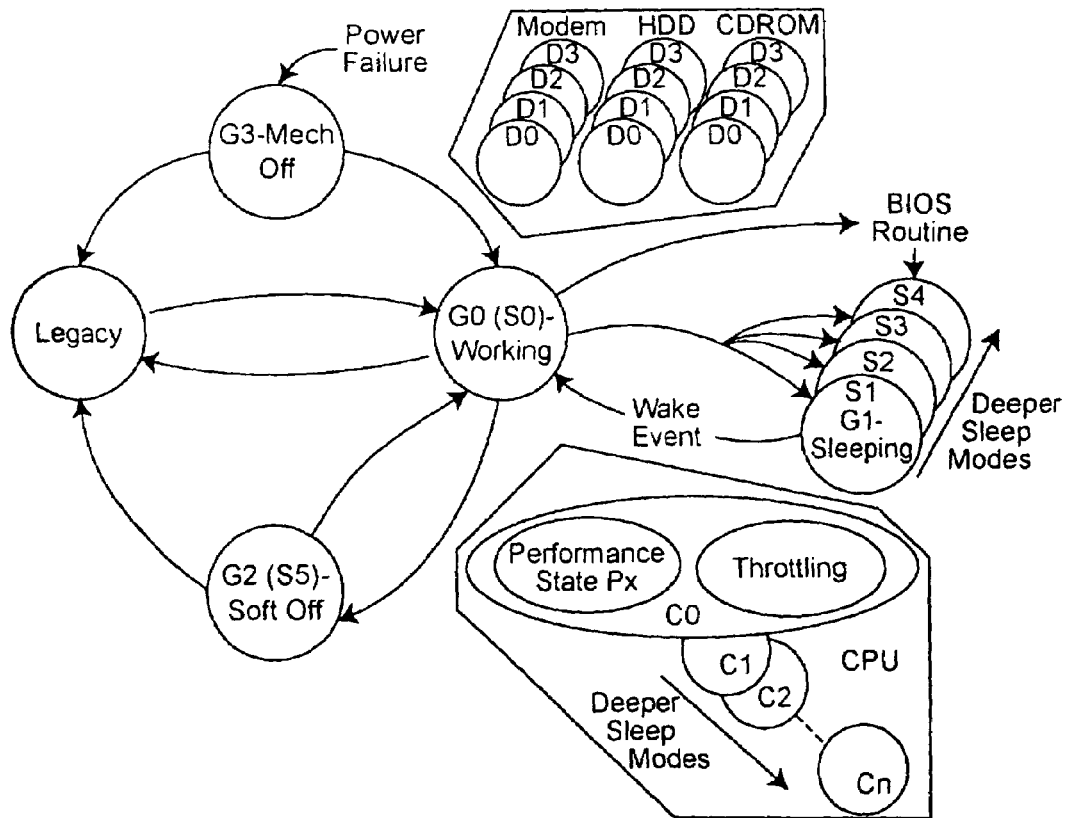


Figure 4

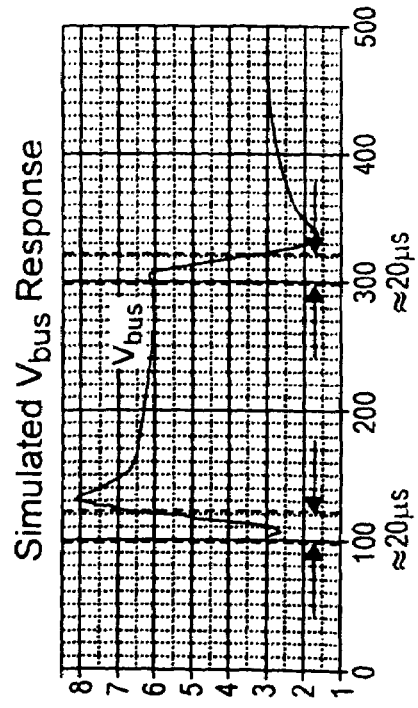
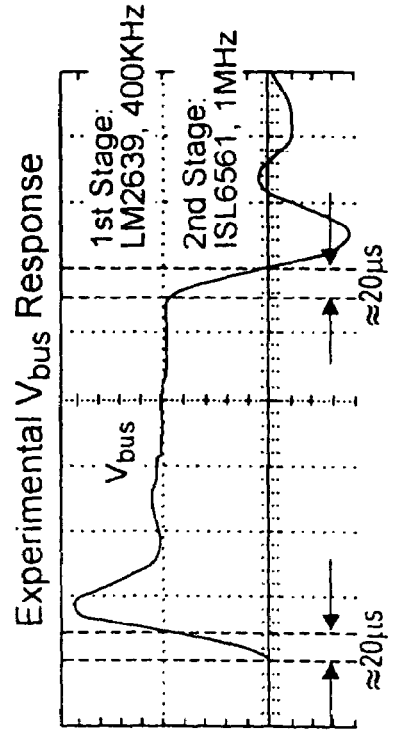
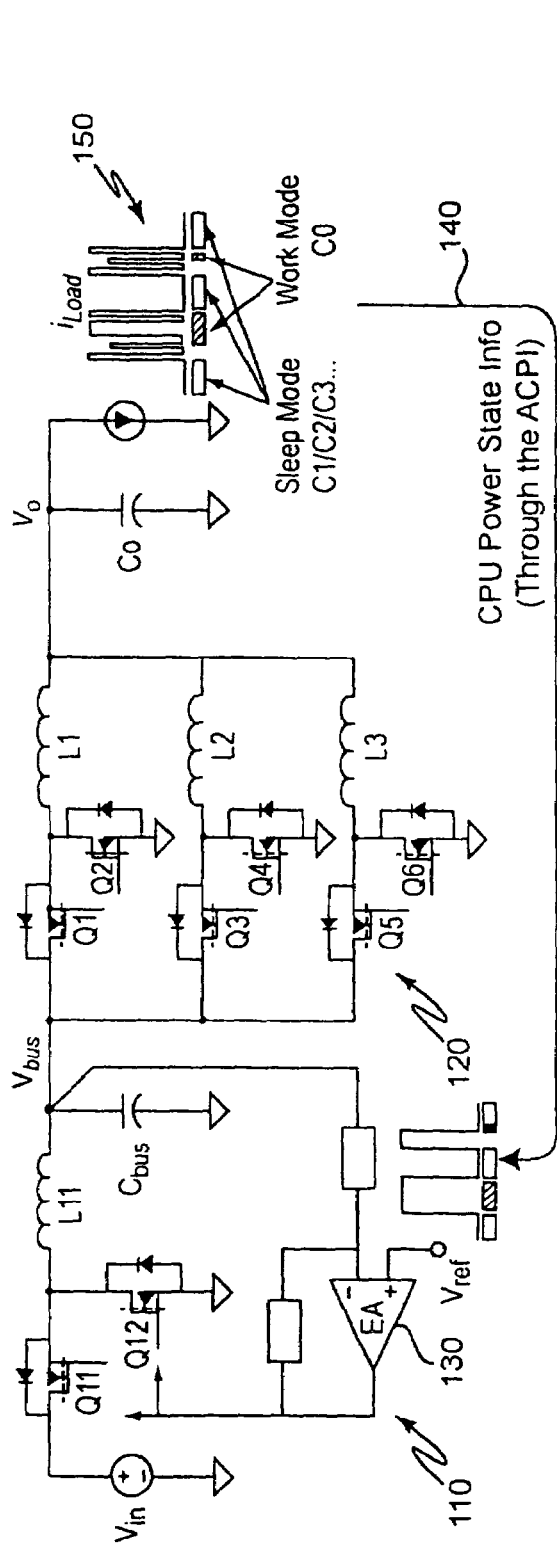


Figure 5

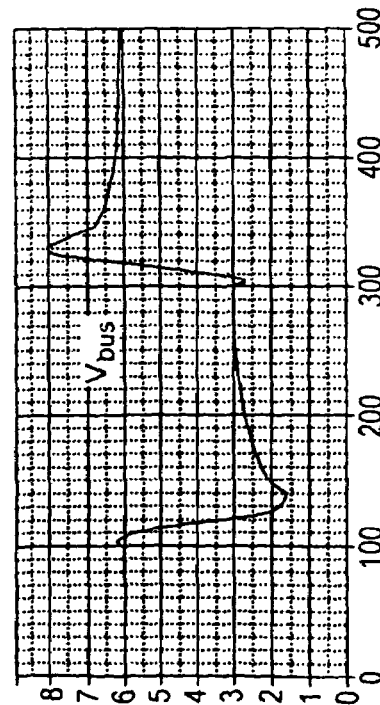
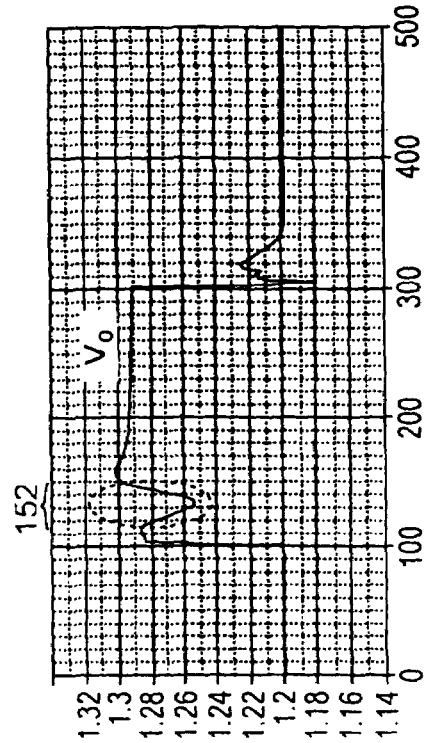
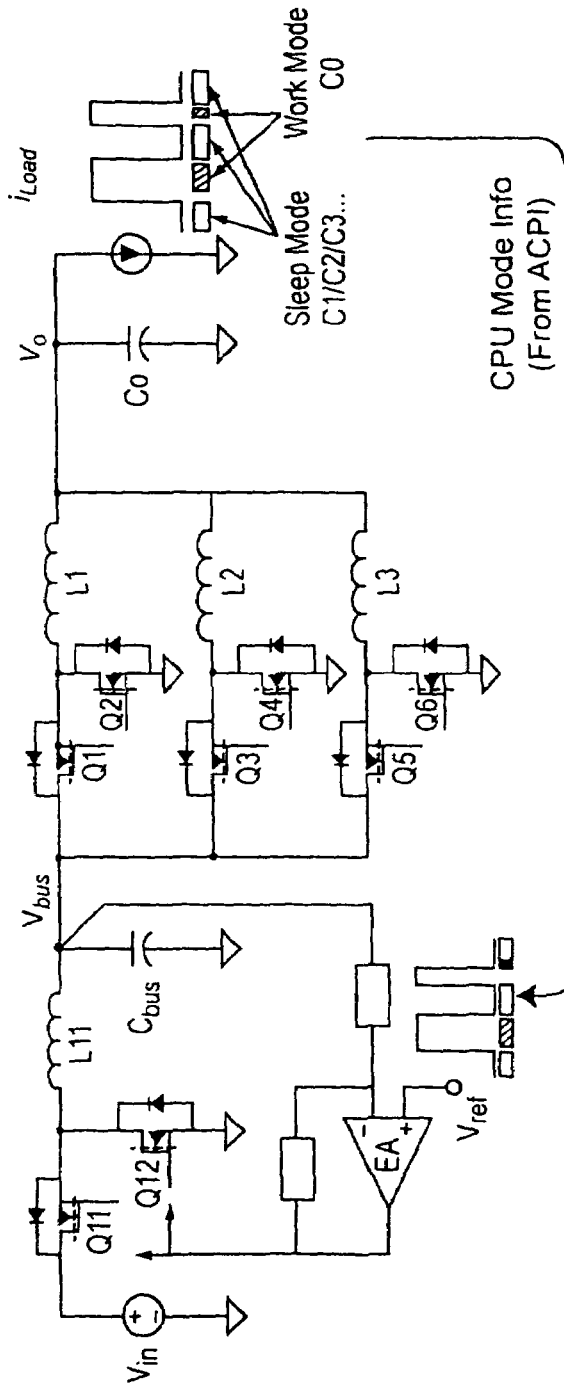


Figure 6

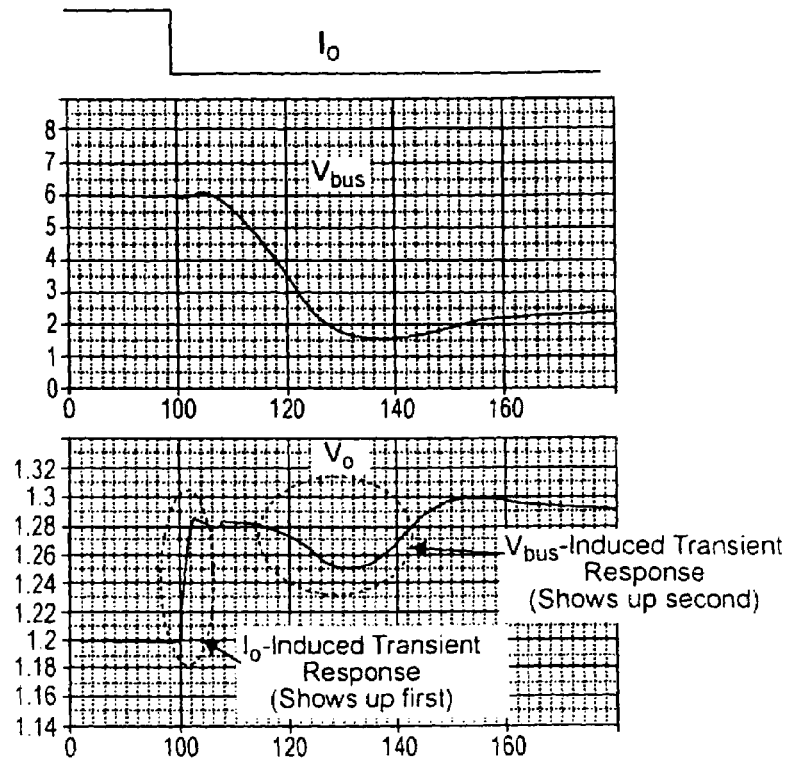


Figure 7

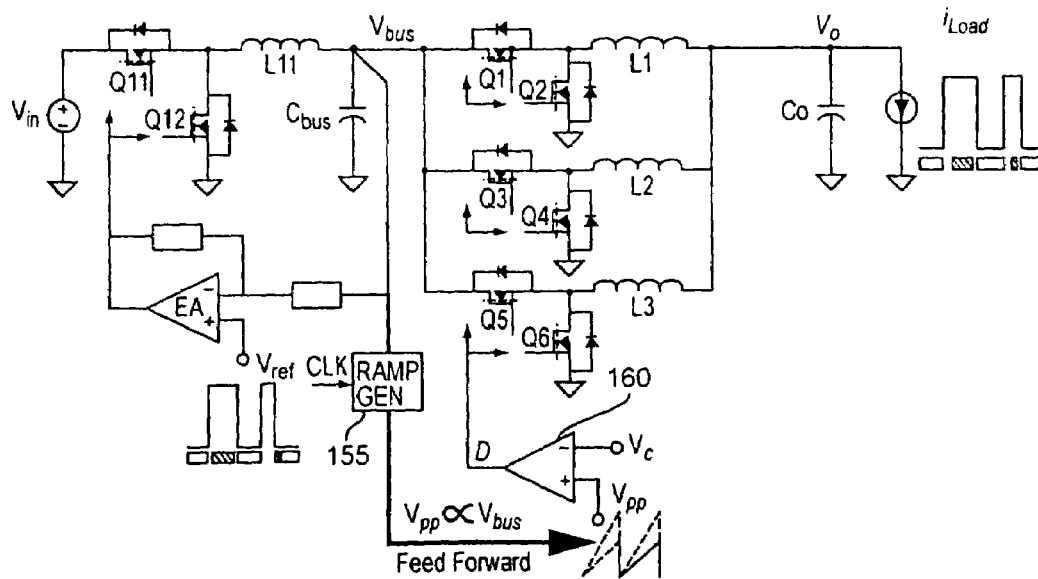


Figure 8

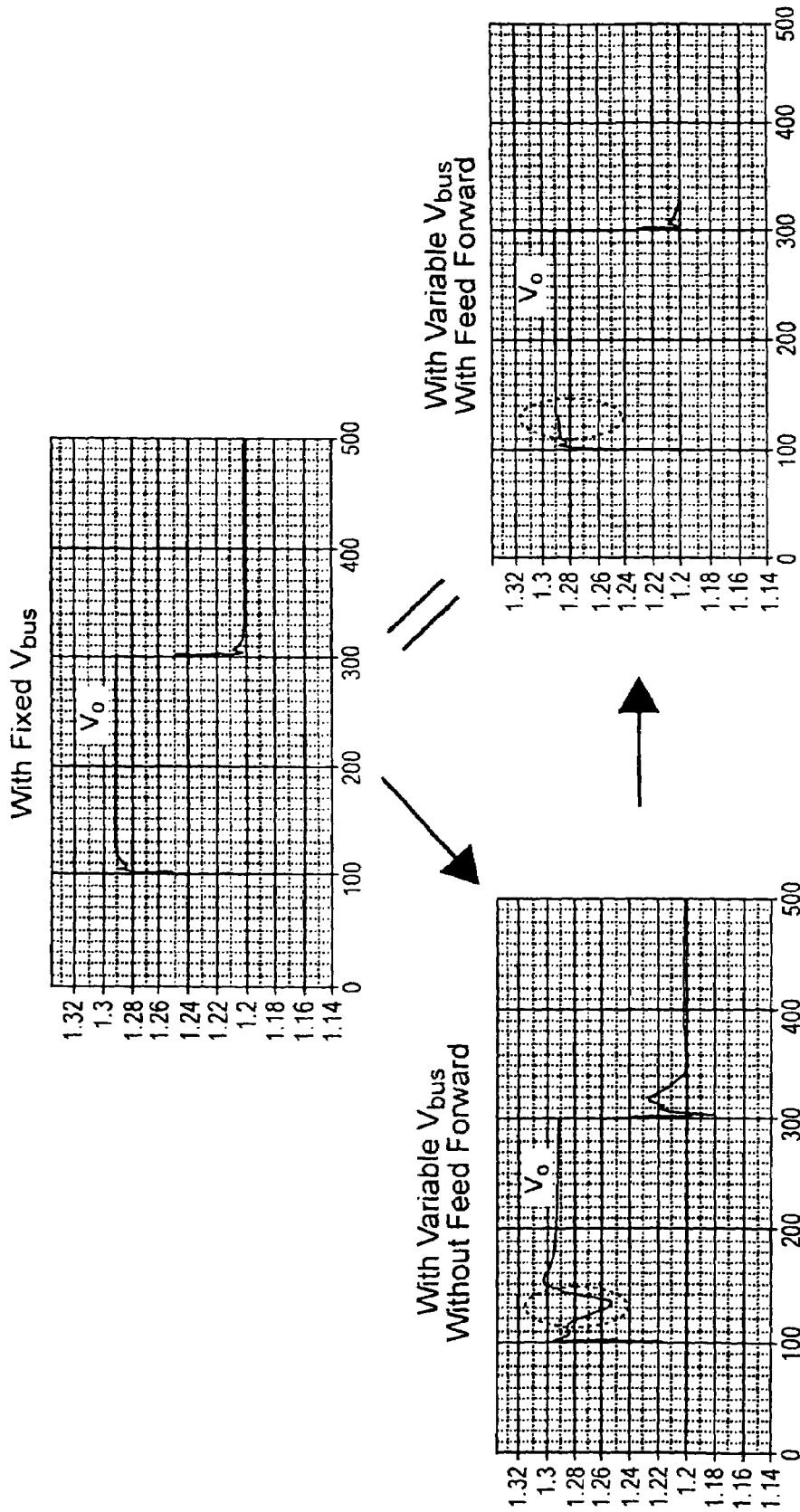


Figure 9

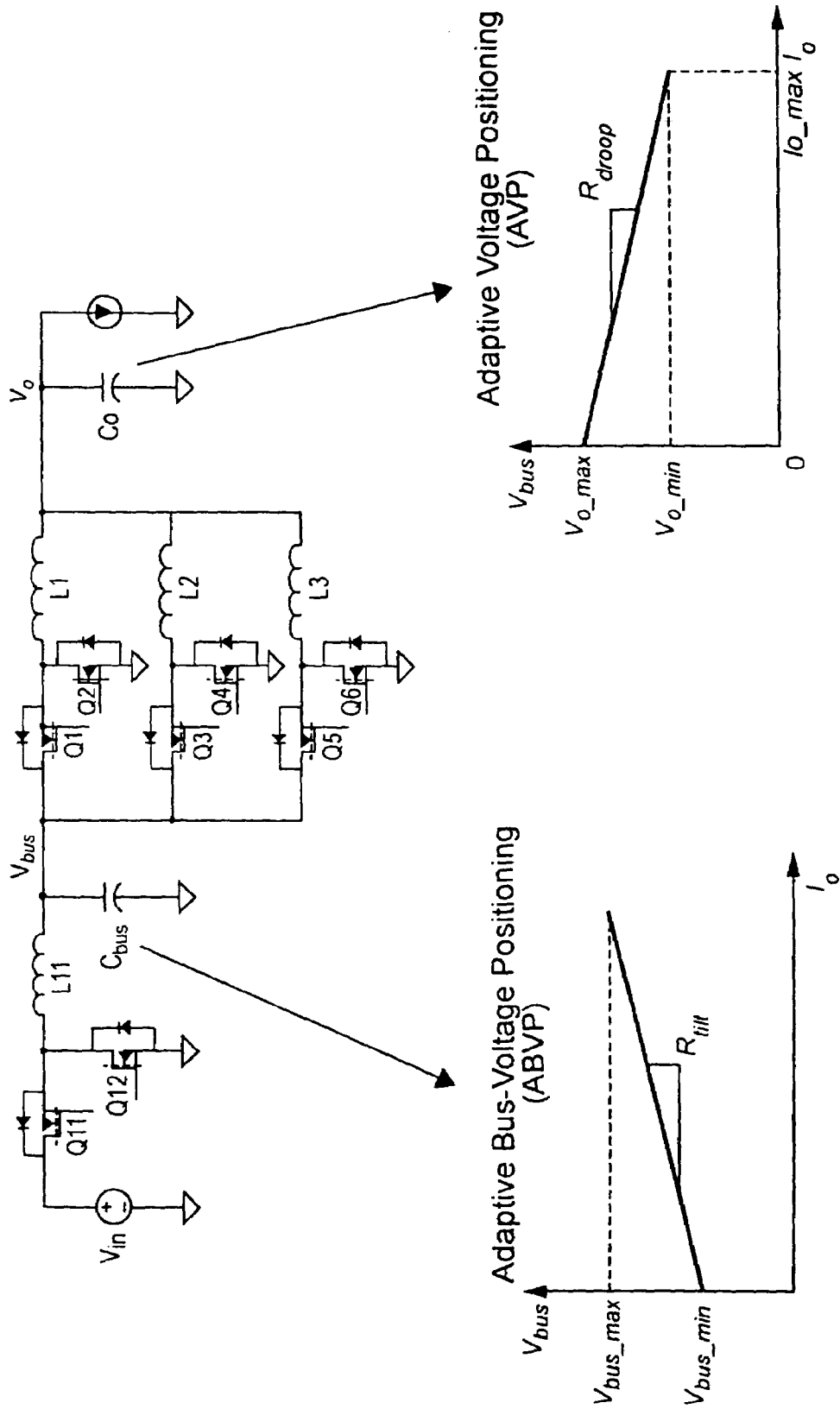


Figure 10A

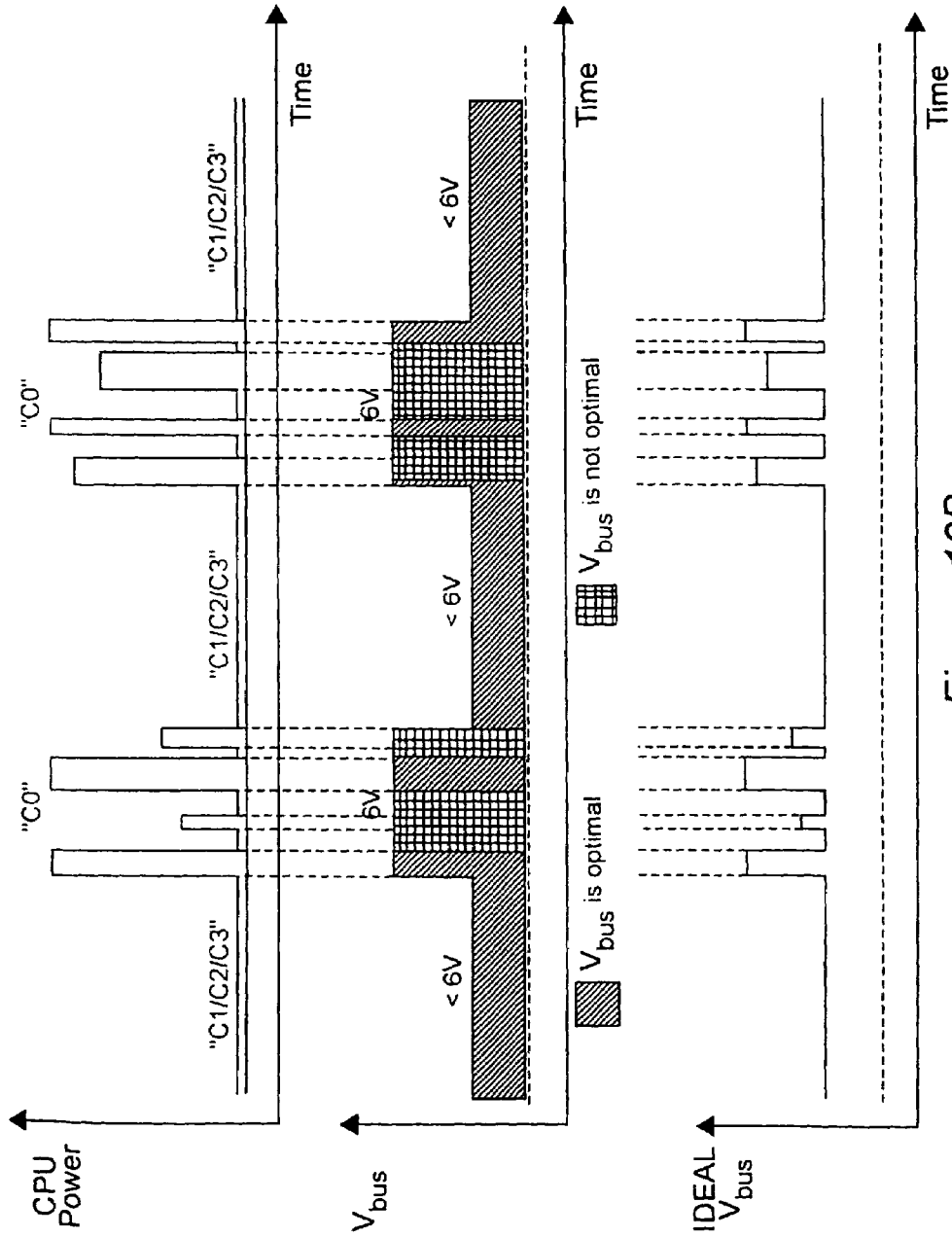


Figure 10B

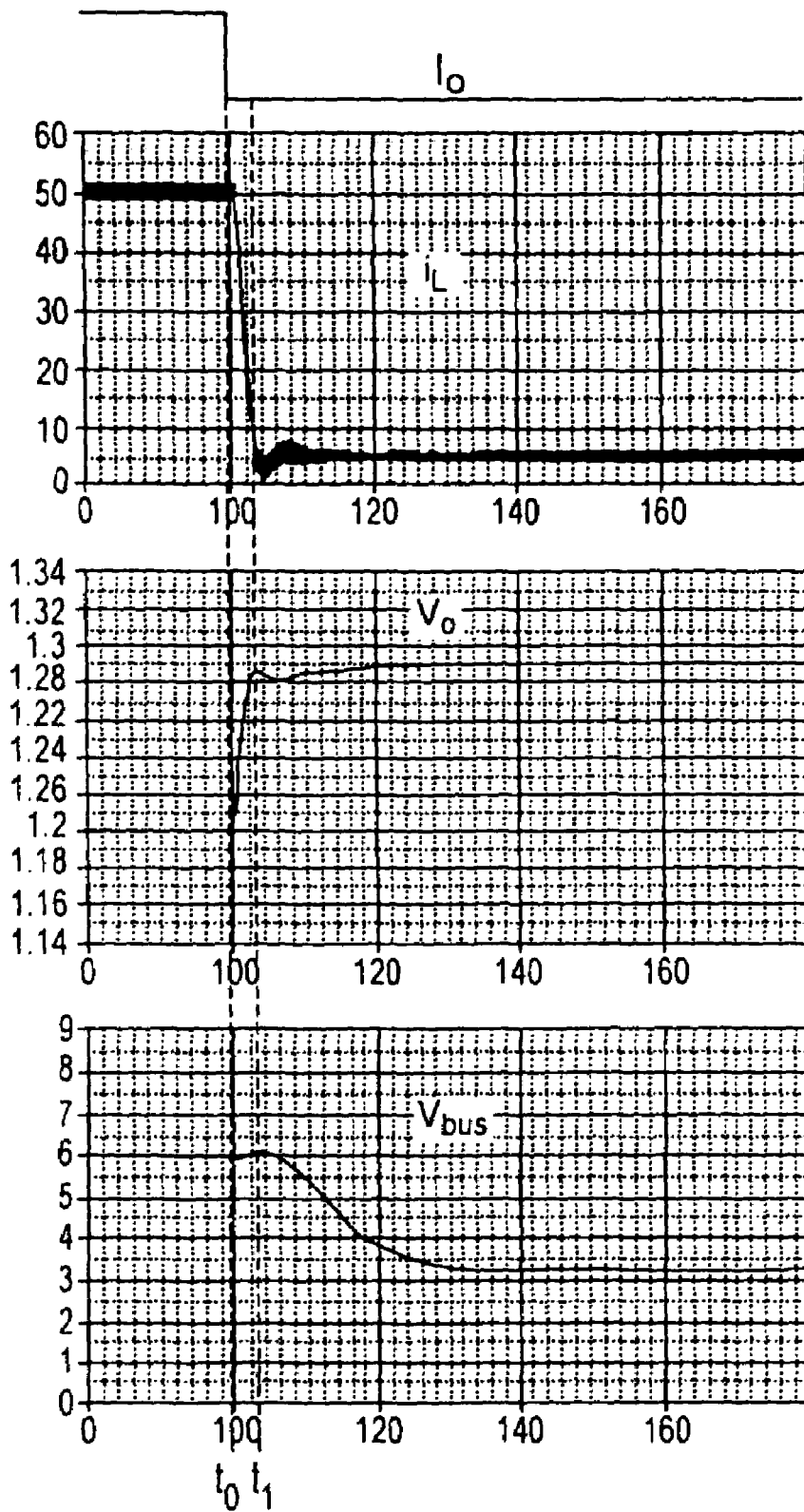


Figure 12

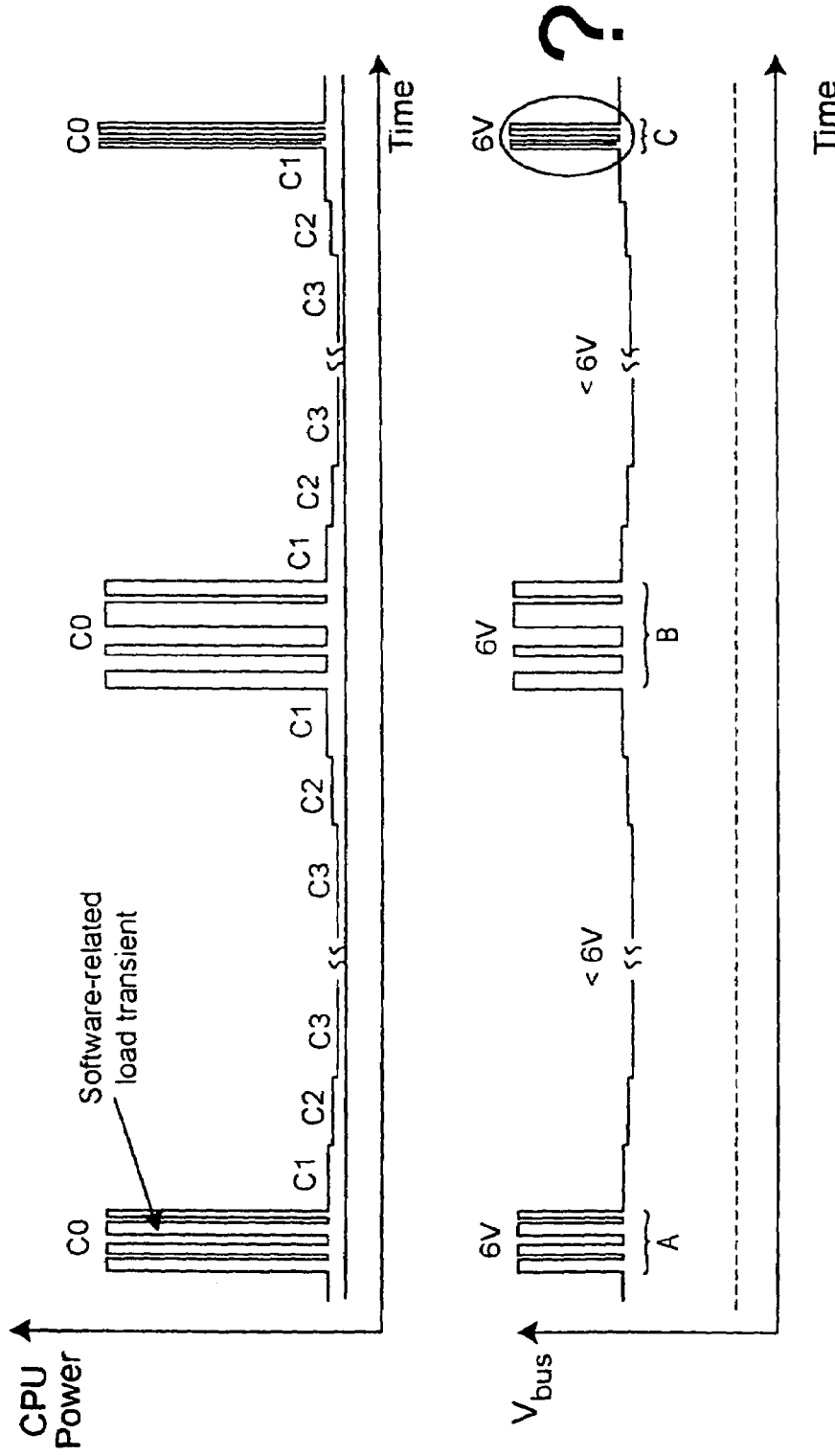


Figure 13

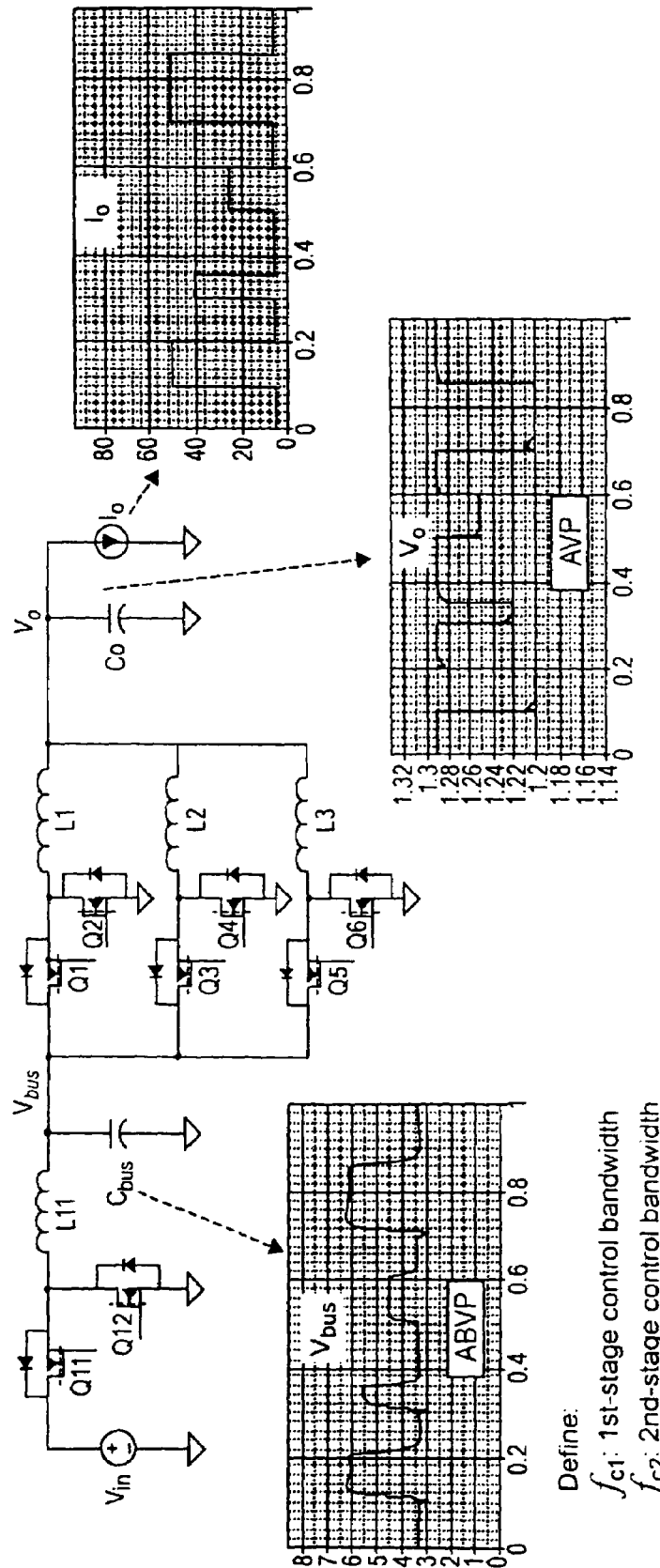


Figure 14A

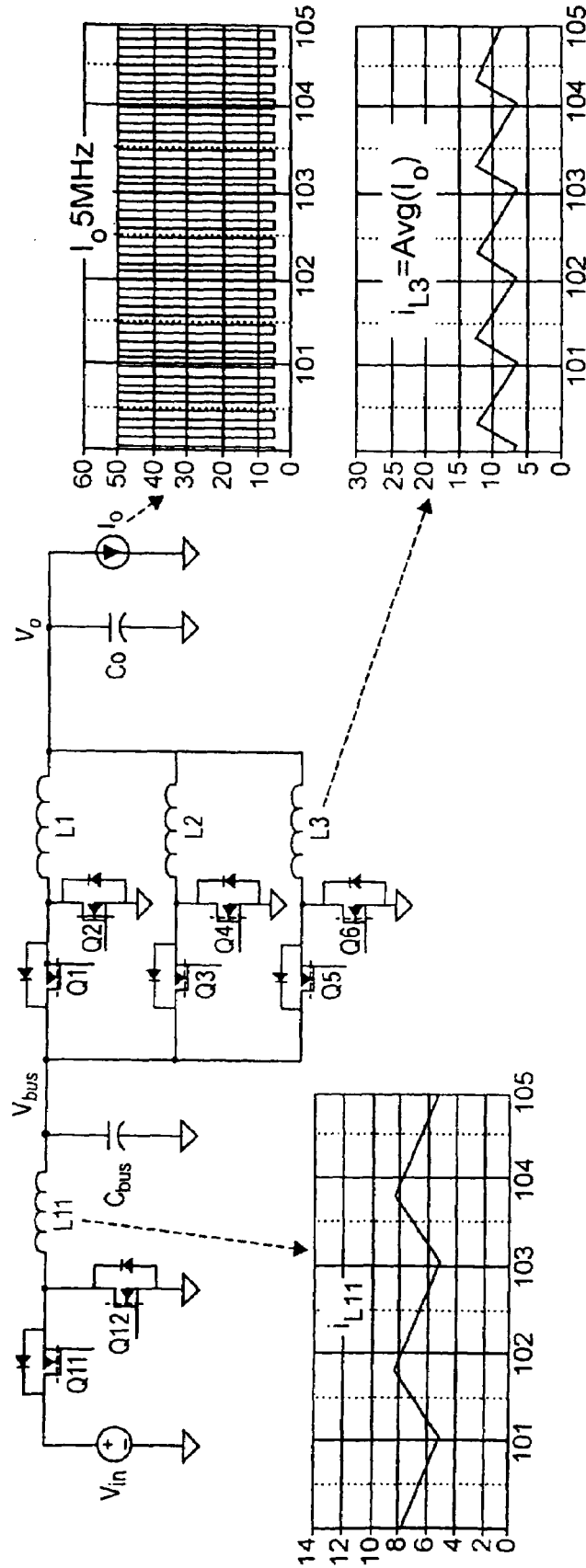


Figure 14B

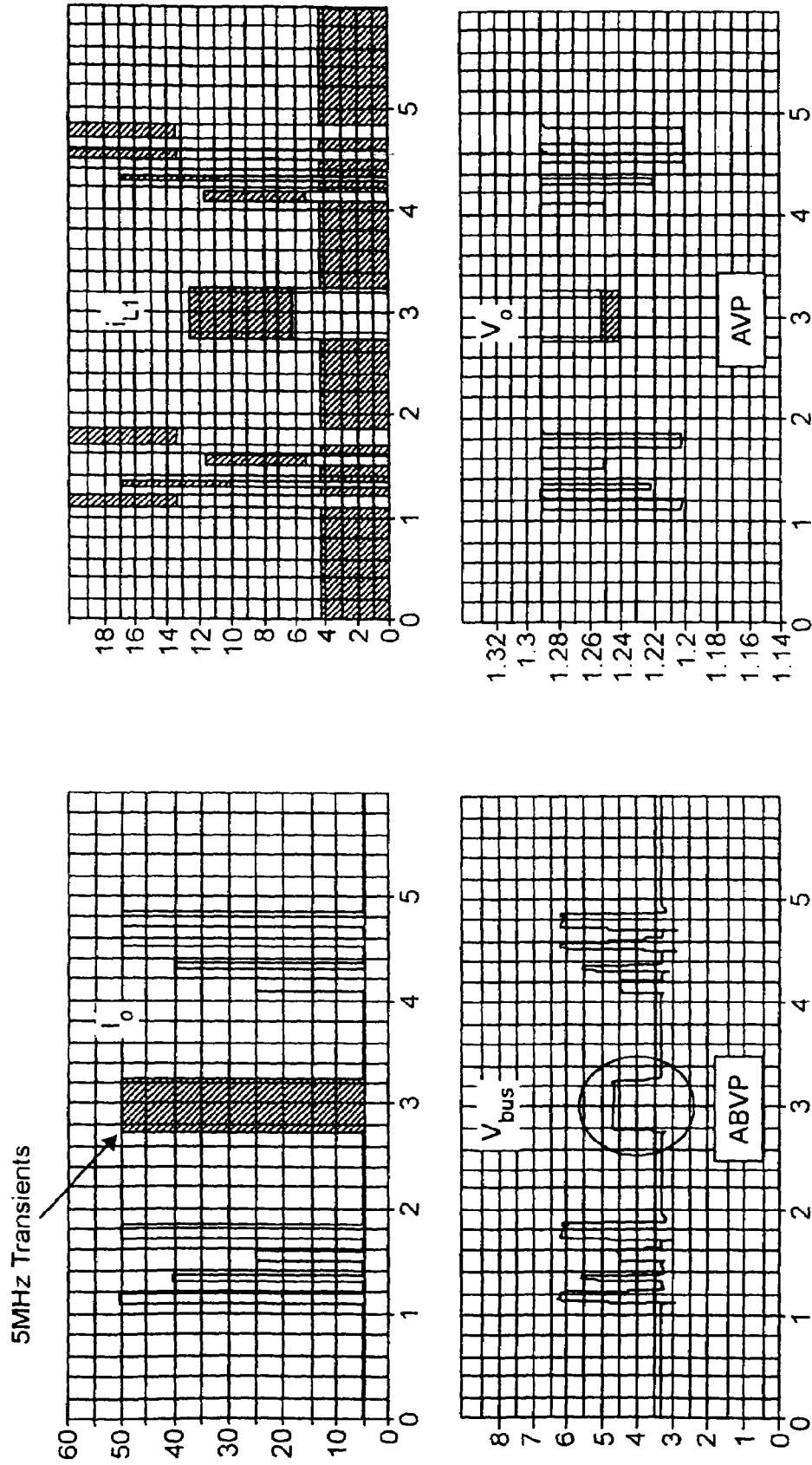


Figure 14C

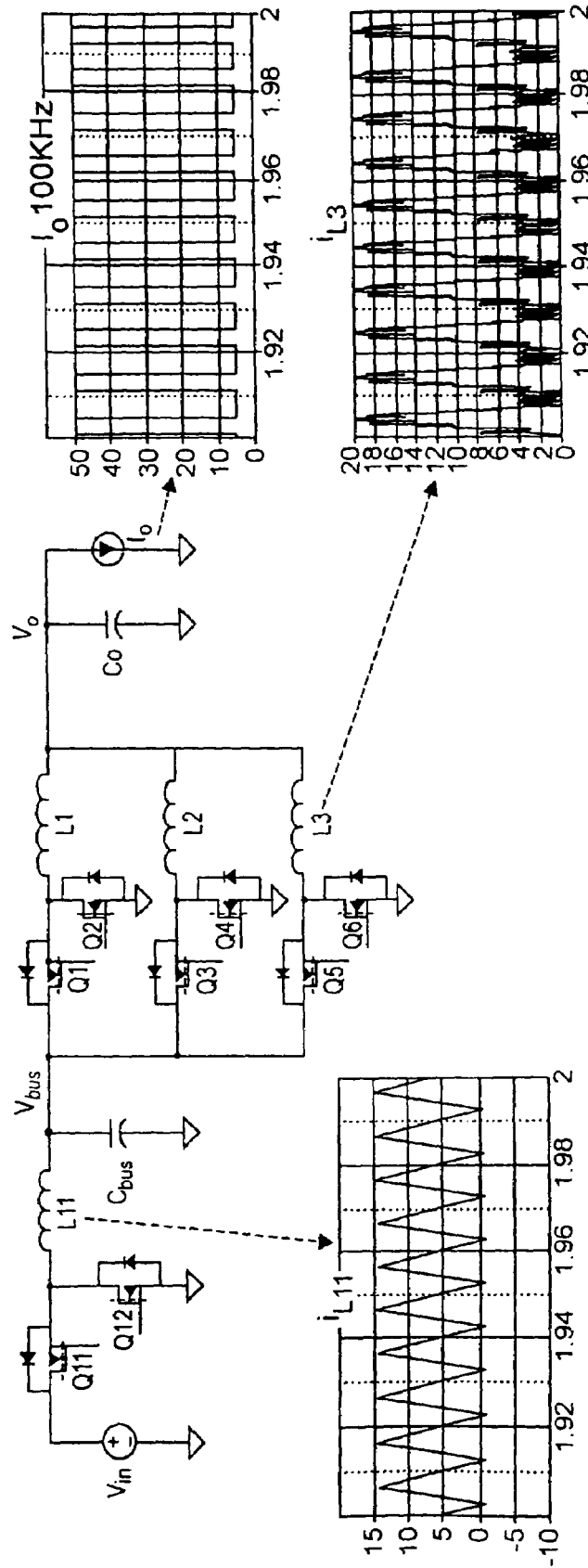


Figure 14D

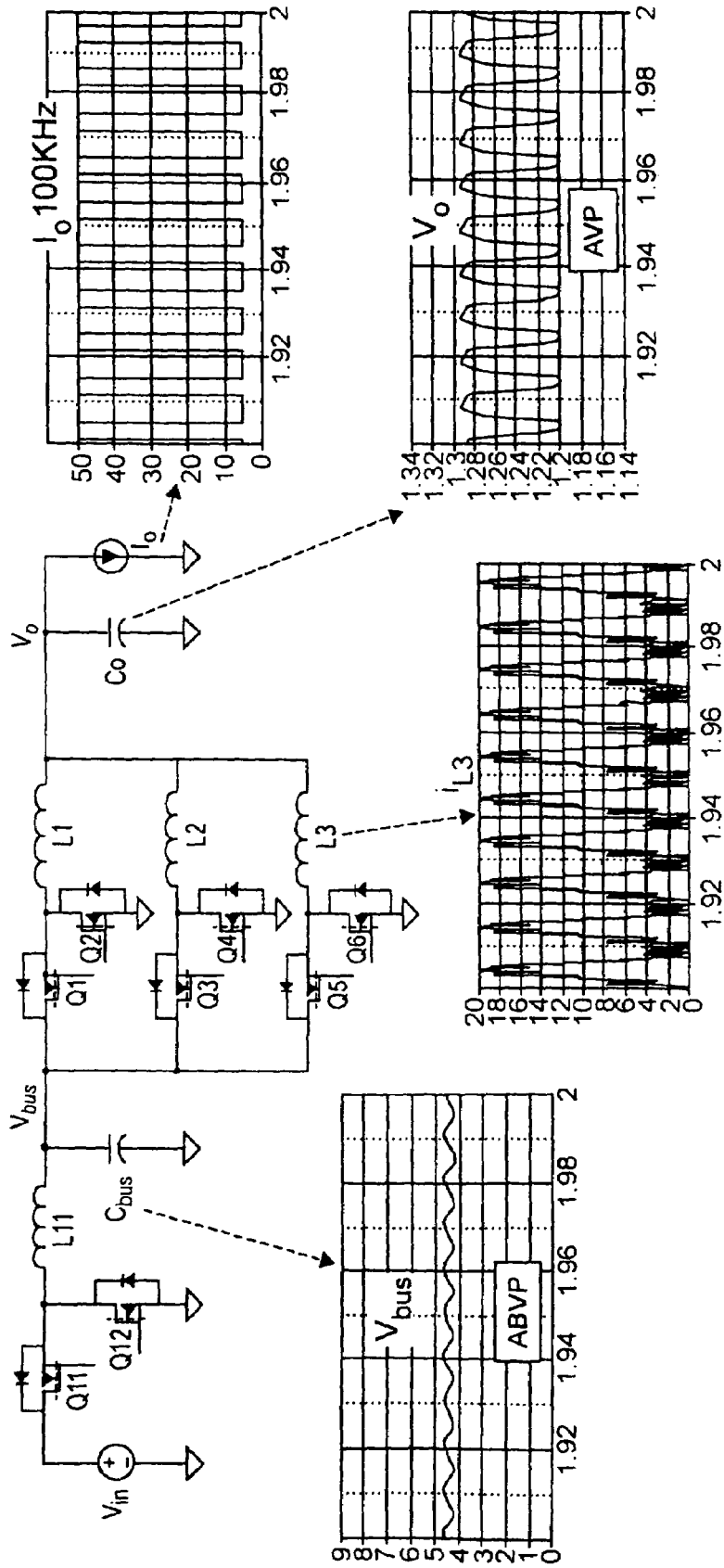


Figure 15

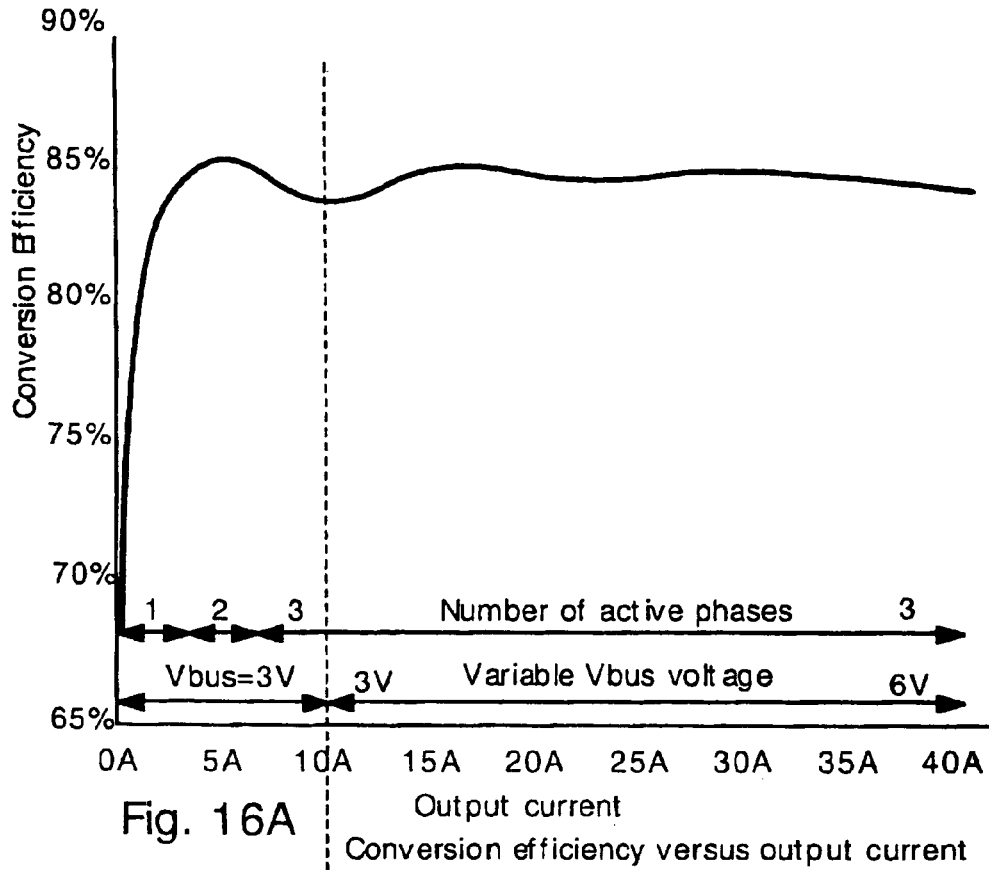


Fig. 16A

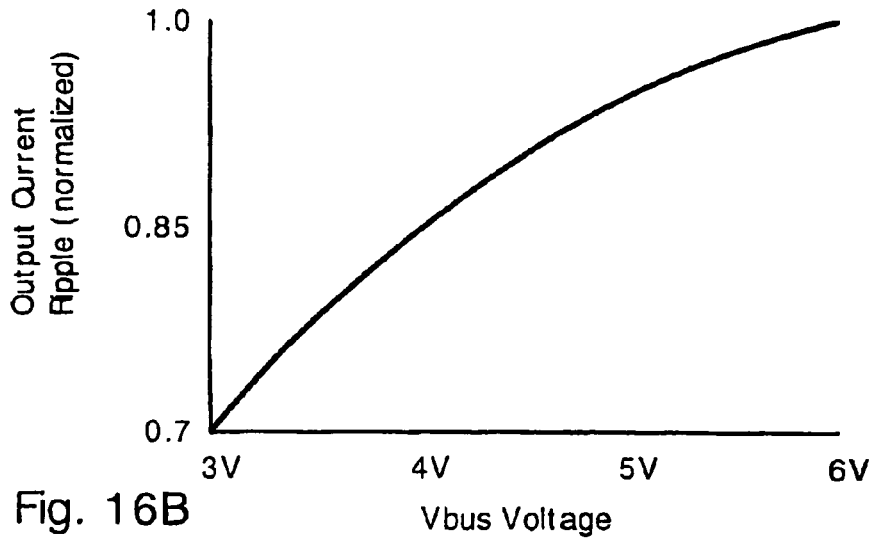


Fig. 16B

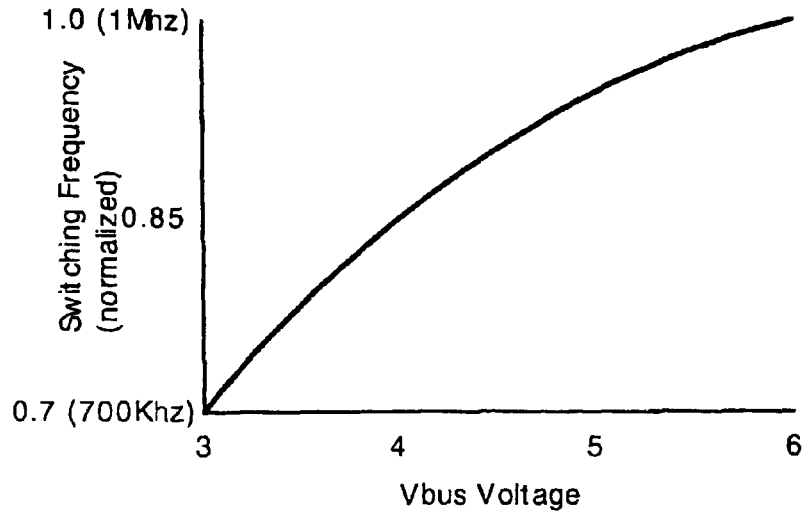
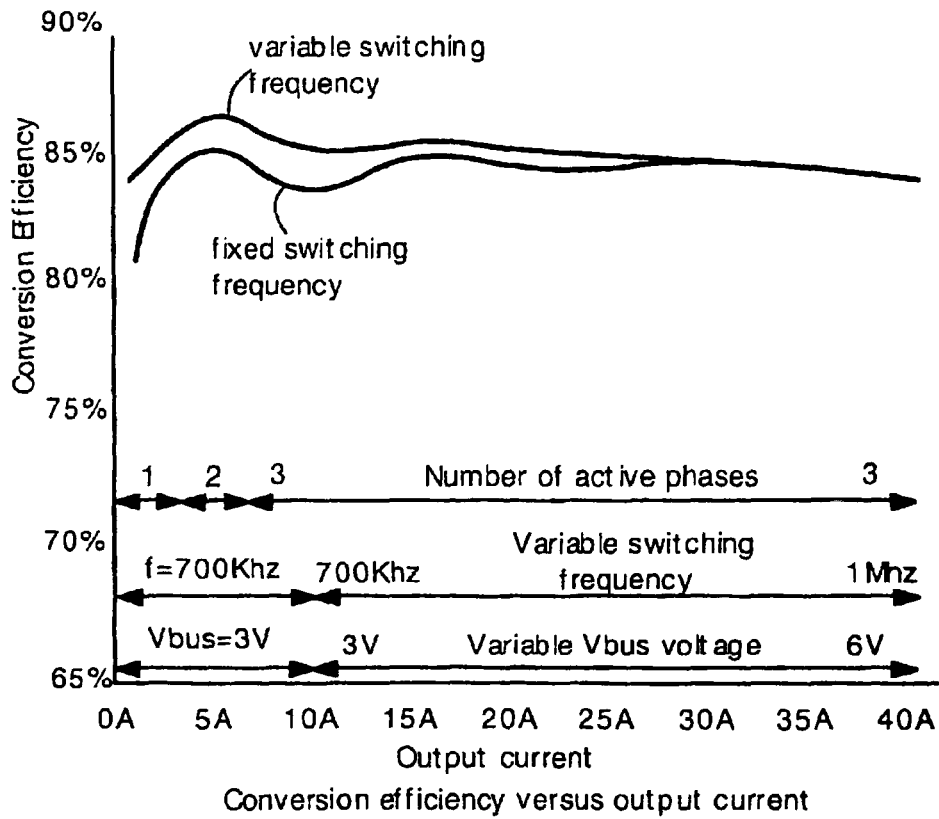
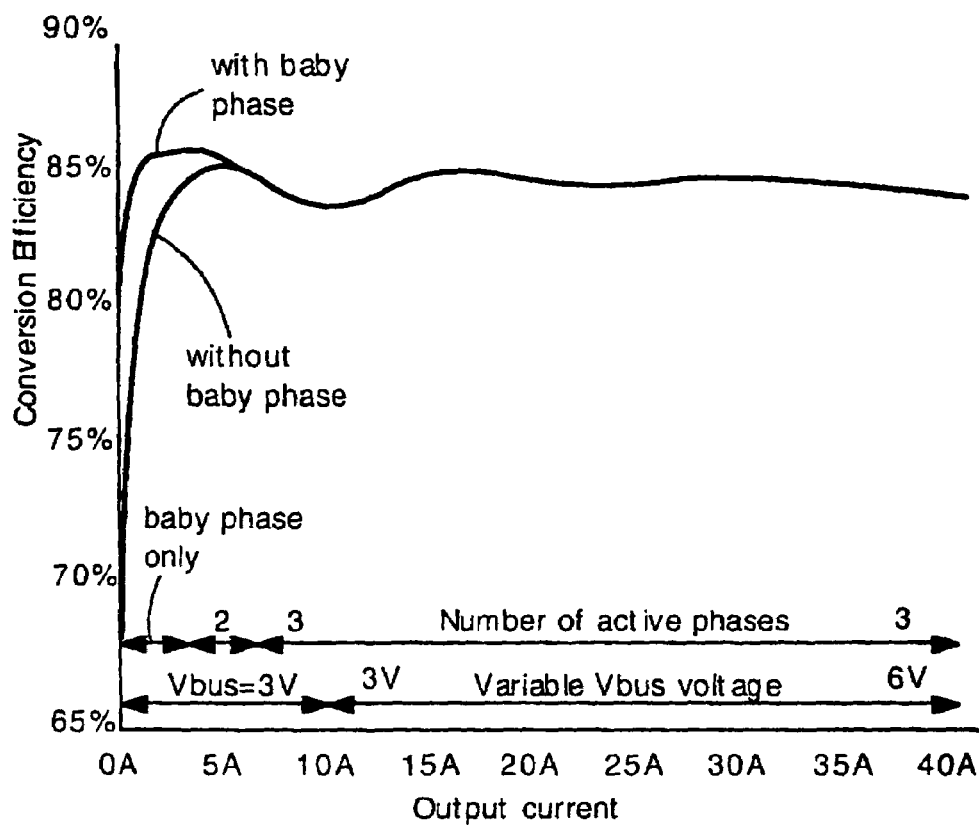


Fig. 17



Conversion efficiency versus output current

Fig. 18



Conversion efficiency versus output current

Fig. 19

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**TWO-STAGE VOLTAGE REGULATORS
WITH ADJUSTABLE INTERMEDIATE BUS
VOLTAGE, ADJUSTABLE SWITCHING
FREQUENCY, AND ADJUSTABLE NUMBER
OF ACTIVE PHASES**

CROSS-REFERENCE TO RELATED
APPLICATIONS

This application is a continuation-in-part (CIP) applica- 10
tion of U.S. patent application Ser. No. 10/781,931 filed Feb.
20, 2004, the complete contents of which is herein incor-
porated by references, and benefit of the priority date thereof
is hereby claimed.

DESCRIPTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to high efficiency 15
electrical power supply voltage regulators and, more par-
ticularly to improving the efficiency of voltage regulators
which must supply power to highly variable loads with
extremely wide variation in current requirements.

2. Description of the Prior Art

All electrically operated devices require electrical power 20
and are designed to operate on the type of power which can
be provided from the source which is most convenient in
view of the intended function. Devices which are generally
operated in a fixed location, such as household appliances
and other devices having moderate power requirements, are
generally designed and constructed to operate on efficiently
transmitted alternating current power of a standard voltage
while larger power requirements may require multi-phase 25
alternating current power at higher voltages. On the other
hand, devices which must be portable for their intended use
generally are designed and constructed to be operated on
direct current from batteries at a nominally constant voltage.

However, the amount of power which may be stored in 30
and recovered from batteries is necessarily limited, particu-
larly where the size or weight of the batteries must be limited
for convenience of the use of the device. Moreover, as a
battery is discharged, the voltage obtainable therefrom nec-
essarily varies and decreases as the battery becomes more
discharged. The internal resistance of batteries, while low in
modern designs, is not negligible and also causes voltage
reduction with increased load. While some devices operat-
ing on battery power may be tolerant of voltage variation,
modern electronic devices using high density integrated 35
circuits, such as may be used in so-called laptop and
palm-top computers and personal digital assistants (PDAs)
which have recently become popular, increasingly require
extremely stable and substantially constant voltage within a
tolerance of a few tenths or hundredths of a volt and thus 40
require high quality voltage regulation.

Unfortunately, circuits capable of regulating voltage, even 45
with relatively wide tolerances, necessarily consume a finite
amount of power since the output voltage must necessarily
be reduced from a higher voltage by causing a voltage drop
across some components in the voltage regulator while a
current is being supplied. The power consumed is thus, at a
minimum, the product of the voltage drop and the current for
analog regulators although such power consumption may be
reduced somewhat by switching regulators as will be disc- 50
ussed below. If the load is relatively constant, the voltage
regulator can be carefully designed to operate with a very

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low voltage drop and thus may be relatively efficient. 5
However, transient changes in load current may cause
corresponding fluctuations in the regulator output voltage
unless the voltage is adequately filtered, generally requiring
a relatively large storage capacitor or voltage regulation
from a higher voltage with a correspondingly larger voltage
drop so that peak currents can be supplied from the voltage
regulator or a combination of both; either of which neces-
sarily requires features which are generally undesirable in a
portable device (e.g. the size and weight of filter capacitors
and the increased inefficiency of the voltage regulator
coupled with increased battery size and weight to compen-
sate for that inefficiency). Further, power consumed by the
voltage regulator must be dissipated as heat in the portable
device and the minimum size and weight of the regulator is
generally increased by both the current which must be
delivered and the heat which must be dissipated. Conversely,
for a given voltage regulator and filter and/or battery size
and weight, the efficiency of any voltage regulator is nec-
essarily reduced in accordance with the magnitude of
changes and frequency of transients in load current it must
accommodate and the accuracy of voltage regulation which
must be provided.

These interrelated problems are particularly acute in 25
regard to portable data processing devices such as laptop
computers and similar device alluded to above. The duration
of operation for each use cycle is generally a significant
fraction of an hour, at a minimum, while digital processing,
memory and logic circuits required therein require
extremely close tolerances of voltage regulation, size and
weight constraints are severe for commercially competitive
designs and, most importantly, the changes in load current
are particularly large, especially in modern processor
designs with sophisticated power saving circuits. More
specifically, modern processors are generally designed to
enter one of a plurality of "sleep states" relatively quickly
when an operation is completed and no new data or com-
mand is entered. Thus, while the peak power requirements
of the processor and associated circuitry may be, for
example, 50 Watts, the average power consumed is a small
fraction of that requirement, for example, an average power
consumption of 5 Watts or less. The duty cycle of the peak
power consumption may be substantially less than ten
percent. Much the same scenario is presented by the display
which generally consumes far more power than the proces-
sor but which may be blanked after a relatively short period
during which the display is unchanged.

Thus, in general and on average, the display represents
about 33% of the power load, the processor represents about
10% of the power load while other associated devices such
as a hard disk storage, clock, memory, modem, network
interfaces and the like, some of which may be intermittent
loads, represent slightly less than half of the power load.
Thus, at the present state of the art, the voltage regulator may
consume an amount of power comparable to that required,
on average, by the processor and is thus a significant factor
in battery life and a significant limitation on the period of
usability of the laptop computer or other portable digital
device per battery charge while the efficiency of the voltage
regulator is generally comparatively lower than for many
other devices in view of the close regulation required and the
wide variation in loads which must be accommodated.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide
a voltage regulator of small dimensions and weight and

having increased efficiency while capable of accommodating wide variation in current load and high frequency load transients.

It is another object of the invention to provide a two-stage voltage regulator wherein the second stage may be of arbitrary design and constitution while the first stage substantially improves overall efficiency of the voltage regulator by providing a variable bus voltage V_{bus} .

The present two-stage converter has a first regulator stage, a second regulator stage and a control circuit that controls the first stage. The first stage provides an adjustable intermediate bus voltage V_{bus} . The second stage receives the bus voltage V_{bus} and provides an output current. The control circuit responds to the output current, and controls the first stage so that the bus voltage V_{bus} increases with increasing output current. This arrangement tends to improve the conversion efficiency.

In a preferred embodiment, a switching frequency of the second stage increases as the bus voltage V_{bus} increases. This tends to further improve conversion efficiency and maintain a constant output current ripple.

Also, in the present converter, the second stage can comprise a plurality of regulators (e.g. buck regulator phases) connected in parallel. The number of active (i.e. operating) regulator phases can be increased as output current increases. This tends to further increase conversion efficiency.

In another embodiment, one of the parallel regulators in the second stage has switches of low current rating (and consequently high switching efficiency). Such a "baby" phase is operable during a very low power mode, which tends to increase conversion efficiency during the low power mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

FIG. 1 is a schematic graphical depiction of an exemplary power consumption pattern in a CPU of a laptop computer,

FIG. 2 graphically illustrates exemplary voltage regulator efficiency for different loads for different intermediate bus voltages,

FIGS. 3A and 3B illustrate a comparison of efficiencies of one-stage and two-stage voltage regulators as a function of load for a fixed input voltage and a variable input voltage, respectively,

FIG. 4 is a state diagram of possible operating states of an exemplary processor device,

FIG. 5 schematically illustrates a generalized embodiment of the invention with simulated and experimental V_{bus} response,

FIG. 6 schematically illustrates a generalized embodiment of the invention as in FIG. 5 with simulated V_{bus} and V_o response,

FIG. 7 graphically depicts the V_{bus} and V_o response of the circuit of FIG. 6 on an expanded time scale,

FIG. 8 schematically illustrates addition of feed-forward to the generalized embodiment of FIGS. 5 and 6,

FIG. 9 graphically illustrates a comparison of the V_o response of a power supply in accordance with the invention with and without feed-forward,

FIG. 10 is a diagram useful in understanding a perfecting feature of the invention in providing adaptive V_{bus} and V_o positioning,

FIG. 11 schematically illustrates a preferred arrangement for providing adaptive V_{bus} and V_o positioning by current injection,

FIG. 12 illustrates design principles of the preferred arrangement for providing adaptive V_{bus} and V_o positioning of FIG. 11,

FIG. 13 illustrates possible variation of load transients in a CPU of a laptop computer,

FIGS. 14A, 14B, 14C and 14D illustrate simulated power supply response of a power supply in accordance with the invention to different recurrence frequencies of load transients, and

FIG. 15 illustrates the high power supply efficiency provided by the invention under mid-frequency power transient recurrence conditions.

FIG. 16A shows a plot of conversion efficiency versus output current for an embodiment having a fixed switching frequency in the second regulator stage.

FIG. 16B shows a plot of output current ripple versus V_{bus} voltage. The output current ripple increases with increasing V_{bus} voltage.

FIG. 17 shows a plot of switching frequency (in the second regulator stage) versus V_{bus} voltage for an embodiment in which the switching frequency is adjusted as V_{bus} voltage changes.

FIG. 18 shows a plot of conversion efficiency versus output current for embodiments having fixed and variable switching frequencies.

FIG. 19 shows a plot of conversion efficiency versus output current for embodiments with and without a "baby" phase in the second regulator stage.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring now to the drawings, and more particularly to FIG. 1, there is shown a graphical representation of an exemplary power consumption pattern for a digital processor through several cycles which each include a plurality of operating states C0, C1, C2 and C3. Operating state C0 is the working state in which the processor is performing data processing operations at the full clock rate. This working state is generally characterized by a plurality of peaks or high plateaus of processing operations interspersed with relatively lower levels of processing and power consumption as may be caused by the software controlling the operations of the processor. The working state periods are generally fairly brief and of variable duration (also dependent upon software) and are usually widely separated (generally due to at least the time required for a user to assimilate the information content of a display of the results of operations during a C0 working period and to provide a further input, requiring further C0 processing). Thus the duty cycle of the C0 working period, while user-dependent, is generally much less than 10%.

In the possibly extended intervals between C0 working periods the processor enters progressively deeper "sleep states" C1, C2 and/or C3 generally depending on the elapsed time prior to another user input or programmed operation; during each of which, progressively less power is consumed by the processor. Each of the "sleep states" generally requires significantly less than 10% of the power required for the C0 state since the average processor power consumed is generally about 10% or less of the peak power requirements. Therefore, it is readily seen that the ratio of peak power requirements and minimum power requirements of a processor substantially exceeds 10:1 and the processor is in

one of the low power sleep state for the predominant portion of the time, often exceeding 90%.

Referring now to FIG. 2 the overall efficiency of a two-stage voltage regulator of a design suitable for delivering a high current over a range of input voltages is illustrated for different current loads I_o . (FIG. 2 includes drive losses associated with driving of the switching transistors such as Q11, Q12, Q1, Q2 in the regulator stages and switching transient suppression. However, since the drive losses are relatively small and do not vary significantly, the trends in the data are the same whether or not drive losses are considered and are not important to an understanding of the basic principles of the invention. Therefore, drive losses will not be further discussed.) For a heavy current load of 25 A and a more moderate load of 18 A the measured efficiency shows a definite peak but at different voltages while for a light load of 5 A, the function is substantially monotonic in the range of interest (a peak would be expected at a lower voltage than is illustrated or practical to utilize in power supplies which must also be able to supply high currents) with higher efficiency being achieved at lower V_{bus} voltage although lower (e.g. 76%) than for the higher current load graphs (e.g. 83%). The V_{bus} voltage yielding maximum efficiency for each current load is depicted by a solid line in each graph with the optimum V_{bus} voltage for a 25 A current load (about 6V) is replicated by a dashed line in the graphs for lower current loads for convenience of comparison. Thus, it is seen that a voltage regulator designed to deliver relatively high current loads tends to have less than optimal efficiency as current loads increase but even greater and highly significant loss of efficiency as current loads decrease, particularly if the voltage, V_{bus} , is held constant (e.g. as indicated by the dashed lines). Therefore, the power requirement pattern for a laptop computer or the like discussed above in regard to FIG. 1 presents several aspects (e.g. high peak current requirements and long periods and high percentage of time in very low power sleep states) which severely compromise overall voltage regulator efficiency. Nevertheless, as observed by the inventors, it is seen that for heavier current loads, a higher V_{bus} voltage yields greater voltage regulator efficiency and for lighter current loads, a lower V_{bus} voltage yields greater voltage regulator efficiency and that V_{bus} can be optimized for different, widely separated load currents for a voltage regulator of substantially arbitrary design.

While this observation underlies a basic principle of the present invention, suitable arrangements for altering V_{bus} to a substantially optimum value based on load is not trivial in practice. Providing switching of regulator input voltages require multiple, separate supplies which would each have significant weight and size. Further, some V_{bus} voltage sources would not be under load at any given time and the voltage delivered is almost necessarily load-dependent and switching from a loaded voltage source to an unloaded voltage source will necessarily involve complications of timing and generation of significant transients in the absence of circuits of substantial size and weight to suppress such transients which, in turn, are likely to compromise overall regulator efficiency in addition to unavoidable loss of efficiency due to the losses and leakage in each of the V_{bus} supplies while unused.

Further, as will be discussed in greater detail below, the inventors have found that an abrupt change in V_{bus} causes an anomaly in operation of a voltage regulator receiving V_{bus} which seriously compromises accuracy of voltage regulation. A solution to this anomaly has been found by the inventors and is discussed in detail below.

As alluded to above, a two-stage configuration is preferred for practice of the invention. This preference is due, in part, to the desirability of providing a generalized arrangement for alteration of the V_{bus} voltage as a first stage so that the invention can be retrofitted to existing voltage regulators to improve overall efficiency, regardless of voltage regulator design or otherwise implemented in existing designs to reduce space, weight and heat dissipation requirements. Further and perhaps more importantly, a two-stage regulator can produce higher efficiency for high current loads than the single-stage regulators which are currently most frequently employed.

It should be understood in connection with the following discussion that switching voltage regulator designs are generally considered to be most efficient and can generally be implemented with relatively few components. Such designs generally employ a switching transistor in series with the input voltage to supply current as needed with a series inductor to smooth the output voltage input to a filter capacitor with a further transistor at the inductor input to reduce switching transients and provide a source of current for the inductor when the series transistor is switched off. In its simplest form, such a circuit is known as a buck converter (since it converts a higher DC voltage to a lower DC voltage and the inductor "bucks" the excess voltage during series transistor conduction) and many variations on this type of circuit are known to those skilled in the art, as are suitable switching control arrangements to obtain a desired voltage. In general, also, when such converters are employed in a two-stage (or multi-stage) voltage regulator, the first stage in generally operated or switched at a substantially lower frequency than the final stage particularly to minimize output voltage ripple while minimizing the size and weight of filter capacitor(s). While such types of switching converters are assumed in the following discussion, it is to be understood that the invention is applicable to any type of regulator circuit(s) but a switching type of converter is preferred as the first stage of the overall voltage regulator circuit in accordance with the invention in which a two-stage arrangement is also preferred.

The relative efficiency of one-stage and two-stage voltage regulators is graphically illustrated in FIG. 3A. The first stage is operated at a switching frequency of 370 KHz using a 2.2 μ H series inductor while the second stage of a two stage regulator or single stage regulator is operated at 1 MHz with a 150 nH series inductor. In other words, FIG. 3 illustrates the difference in performance attributable to the addition of a first stage. It will be observed that at current loads below about 4 A, the efficiency is substantially identical with the single stage regulator having slightly increased efficiency from about 4 A to 8 A load. At higher current loads to 45 A, the two-stage regulator is significantly more efficient with comparative efficiency increasing for the two-stage regulator with increasing current load (e.g. substantially constant efficiency near 85% while the efficiency of the single-stage regulator only slightly exceeds 75% and declines slightly with increasing load). It should be appreciated that the slight advantage in efficiency of the single-stage regulator at loads of about 5 A (the average current load for a processor, as discussed above) together with the low duty cycle or percentage of time the processor requires much higher current loads as well as the slight simplification and reduction of parts count may account for the current common usage of single-stage voltage regulators in laptop computers notwithstanding the significantly lower efficiency at higher current loads (where the regulator losses are nearly doubled) and the substantially identical performance at

current loads below 4 A characteristic of most current processor sleep states and which must be the case to cause the average load to fall to 5 A or less. This rationale also neglects consideration of the fact the V_{bus} will be transiently altered in single-stage regulators upon switching to or from high current load periods; further decreasing efficiency by reducing V_{bus} during the early portions of high current load and increasing V_{bus} during early portions of low current load.

FIG. 3B illustrates the improvement in voltage regulator efficiency (here omitting drive losses) of two-stage regulators attributable to use of variable V_{bus} voltage as compared to the same voltage regulator circuit where V_{bus} is fixed. The voltage regulator circuit and V_{bus} (=6V, similar to FIG. 2) are optimized for a current load of 45 A and the efficiency curves illustrated converge at that load. For the variable V_{bus} curve, V_{bus} varies between 3V and 6V over the range shown and a substantial difference in efficiency is evident near and below the bottom end of this range as V_{bus} is reduced from 6V to 3V.

As illustrated in FIG. 3B, V_{bus} remains constant (at about 3 volts) when output current is below 10 A. In the present invention, in order to increase the conversion efficiency in the low load regime (less than 10 A), the number of operating (active) phases (illustrated as 1 ϕ , 2 ϕ , 3 ϕ which indicate one, two or three operating phases, respectively) is varied according to output current. This aspect of the invention is also illustrated in FIGS. 16A and 18, which show the number of active phases as a function of output current (assuming a total of three phases). At very low output current (e.g., less than 4 amps), only one phase (e.g. buck regulator phase comprising switches Q1 Q2 in FIG. 5) is operating. As output current increases (e.g., in the range of 4–7 amps), a second phase (e.g., buck regulator phase comprising switches Q3 Q4 in FIG. 5) is activated. As output current increases further, the third phase (e.g., buck regulator phase comprising switches Q5 Q6 in FIG. 5) is activated. The three phases are connected in parallel, so their output currents add. Since switching losses dominate in the low output current regime, minimizing the number of operating phases tends to increase efficiency. Hence, adjusting the number of active phases provides the large increase in operating efficiency (about 5–15%) in the low output current regime (less than 10 A), as illustrated in FIG. 3B.

The present invention includes embodiments where the second stage comprises multiple regulators (phases) connected in parallel, with the number of active regulators increasing with increasing output current (as described above). Preferably, as illustrated in FIGS. 5, 6, 8, 10A, 11, 14A, 14B, and 15, the second stage comprises multiple buck regulators connected in parallel. The number of parallel regulators in the second stage can be 2, 3, 4 or more.

In a preferred embodiment of the invention, the V_{bus} voltage is varied only when all the second stage regulators are active.

The multiple regulators or phases can be operated in phased relation. For example, if 3 phases are employed in the second stage, as illustrated in FIG. 5, the phases can be operated with a 120 degree phase lag between each. Similarly, if 4 phases are employed, then the phases can be operated with a 90 degree phase lag between each. Phased operation of multiple switching or buck regulators is well known by those skilled in the art.

In another aspect of the invention, one of the secondary regulator phases (e.g. phase comprising switches Q1 Q2 in FIG. 5) is constructed with switches that have exceptionally low current handling capability, and consequently, excep-

tionally low switching losses. Such a ‘baby phase’ can be used to provide increased efficiency in the very low output current regime. FIG. 19, for example, shows a plot of efficiency of a multiple phase buck regulator where the first-activated phase (baby phase) has switches with a current handling capability of about $1/10$ that of the other phases. Since the baby phase has exceptionally low switching losses, it is designed for low power/low current operation, and it tends to increase efficiency in the low current regime. In this embodiment, the switches in the baby phase should have a current rating that is $1/5$, $1/10$ or $1/20$ the current rating of switches in the other phases. For example, the baby phase can have switches rated for about 2 amps, and the other phases can have switches rated for about 20 amps. The baby phase can be active or inactive when the regulator is supplying high current and the other phases are active. The baby phase can be a buck regulators or other kind of voltage regulator.

To convey a more complete understanding of the exemplary power requirement profile of a laptop computer or the like as depicted in FIG. 1, an exemplary state diagram of such a device is depicted in FIG. 4 as generally implemented by an Advanced Configuration and Power Interface (ACPI) developed by a number of commercial CPU manufacturers. (The prefix “G” is used to connote “global” while the prefix “C” is a specific reference to the CPU state. Prefixes “D”, “P” and “S” are specific to other devices in the computer or the like. Numbers refer to particular states of the global system or respective devices with “0” representing the working state and higher numbers representing progressively deeper sleep states with progressively lower power requirements.) This state diagram can possibly be best considered as excursions away from and back to the C0 working state operation of the processor and peripheral devices begins with the G3 mechanically off state (which can be re-entered by a power failure to invoke the G0(S0) state to initiate, for example, a shut-down procedure to avoid data loss or corruption and a similar action in legacy systems). When the system is mechanically switched on, the processor enters the G0 working state to execute the BIOS routine before entering a sleep state G1 which may include any of a plurality of sleep states (here illustrated as S1–S4) which differ in the amount of active processing logic and the like and corresponding amount of required power therefore. A wake event, such as a keyboard entry, returns the processor to the G0 state. An even deeper sleep state is depicted as G2(S5) which is a “soft off” state entered after a given period of another sleep state through the working state so that data loss or corruption or other errors or malfunctions can be avoided when in an extreme low power mode in the processor and legacy systems. The working state C0 and sleep states C1–C3, referred to above in regard to FIG. 1 correspond to combinations of the processor working state, G0(S0), or sleep states, G1(S1–S4) or G2 (S5) and various active or standby states, D0–D3) of peripheral devices or legacy systems as depicted in the insets of FIG. 4.

It should be appreciated that changes of processor state are known in advance by and through the processor, itself. More specifically, C0 is the heavy load performance state although a percentage of maximum performance is generally controlled for battery life and thermal considerations and is generally referred to as “throttling”. C1–Cn are light load sleep states. All transitions between the C0–Cn states are possible (e.g. C2–C0, C0 to C1, C2 or C3, etc.) controlled by an Operating System Power Management (OSPM) system running in the CPU. The C1 state is generally indicated through a dedicated processor pin (e.g. the “HLT” pin for

Intel 32-bit CPUs). The C2 and C3 states are generally entered by using the P_LVL2 and P_LVL3 command registers or the like, respectively, and similar operations may be provided for other possible sleep states. The Operating System Power Management (OSPM) system controls transitions between different modes and the CPU is aware of a transition generally at least 20 μ sec (and often much longer) before the transition is to occur. Moreover, entry into or exit from sleep states C1, C2 or C3 requires some degree of hardware latency. The latency is declared in a Fixed ACPI Description Table (FADT). However, the variations in load during the C0 CPU state are not controlled by the OSPM, are totally unpredictable and may occur in the MHz range under processor clock control and thus cannot be followed by a practical voltage regulator. It is also possible for some momentary high current CPU requirements to occur outside the C0 state which also cannot, as a practical matter, be predicted or tracked by a practical voltage regulator.

Thus, in accordance with the invention in its most basic form, it is proposed to provide a higher nominal V_{bus} voltage (e.g. 6 volts) for the C0 state and lower nominal V_{bus} voltage (e.g. 3 volts) for the sleep states; both as indicated through the ACPI in view of the large difference in current requirements between the operating state, C0 and the sleep states, C1–Cn, and the relatively small difference in current requirements of the respective sleep states. It is also preferred in accordance with the basic form and first embodiment of the invention to position V_{bus} to discrete voltage levels in response to the ACPI rather than measured current requirements to more accurately synchronize the change of V_{bus} between discrete voltage levels with the CPU operating state although adaptive adjusting of discrete V_{bus} voltage levels in accordance with a perfecting feature of the first embodiment of the invention or adaptive positioning of V_{bus} over a continuous range of values (e.g. without providing discrete V_{bus} voltage levels as in the second embodiment of the invention) could be provided based on other measured or predicted information including measured load current. It should also be understood that more than two discrete, nominal V_{bus} voltage levels could be provided in the first embodiment of the invention if justified by the power consumption pattern for a particular device (e.g. other than a CPU) to be powered. On the other hand, it is considered by the inventors that, at least for different loads required by a CPU or the like, provision of other voltages through adjustment of either of two nominal (operating state responsive) V_{bus} voltages in a manner which is responsive to measured current, as will be described in detail below as a perfecting feature of the first embodiment, is preferable to providing additional discrete nominal V_{bus} voltage levels and provides additional efficiency, as well.

Referring now to FIG. 5, a two-stage voltage regulator in accordance with a preferred form of the basic invention is depicted schematically. The first or V_{bus} supply stage is indicated at 110 and the second stage indicated at 120. The circuits in the first and second stages include, for example, a plurality of switched buck regulator circuits of a known type as discussed above and it is to be understood that the invention is not limited to such circuits but other regulator circuit configurations may be used. The second stage includes a plurality of such circuits connected in parallel and operating at high frequency of different phases, as is also known in the art for high current supply capability. It is considered to be preferable that operation of some of these parallel regulator circuits may be selectively discontinued based on load current requirements, particularly at low current level loads. This illustrated embodiment of the

invention differs from the voltage regulator circuit commonly used in laptop computers and the like at the present time by being configured as two stages and having a feedback loop with a voltage comparator 130 in the first stage to control the first stage switching and thus control the V_{bus} voltage and which also provides for a feedback signal 140 from load/CPU 150 which indicates its power state through the ACPI (indicated in FIG. 5 by shading for sleep modes C1–C3 and solid for work mode C0). Thus, the switching times of transistors Q11 and Q12 can be controlled to alter V_{bus} as indicated graphically in FIG. 5 from, for example, 3V to 6V.

Preferably in accordance with this basic embodiment of the invention, there is no repositioning of V_{bus} for the duration of any particular CPU state and the V_{bus} response is rapid and within the period of hardware latency for state transitions alluded to above. Further, since the feedback 140 is through the ACPI which has advance information concerning any change of CPU power state, the change of V_{bus} may be initiated somewhat in advance of the actual CPU state change and thus closely synchronized with changes in the current requirements of the load.

It was noted above, however, that the inventors have discovered an anomaly in the performance of this arrangement which somewhat compromises the accuracy of voltage regulation and may engender transients and possible errors or malfunctions in the CPU. Specifically, the change in V_{bus} voltage must be fairly substantial to optimize V_{bus} for widely differing or varying current loads as discussed above particularly in regard to FIG. 2. When a substantial change in V_{bus} is made, a spike appears in the regulator output voltage V_o as shown at 152 of FIG. 6. This anomaly is basically due to the necessarily or at least highly desirable difference in operating frequency or control bandwidth and, hence, transient response between the first and second stages of the voltage regulator and has not been previously recognized or addressed, particularly since increase of voltage regulator efficiency by positioning of V_{bus} has not previously been provided.

More specifically, as illustrated in FIG. 7, the V_{bus} response of the first stage is dominated by the first stage control bandwidth. The second stage V_o response has two components: the I_o induced transient response (e.g. the output impedance induced voltage change when the load increases or decreases) and the V_{bus} -induced transient response. Essentially, the I_o induced transient response appears first in the second stage prior to the change in V_{bus} . The change in V_{bus} then causes a transient but significant change in V_o following the I_o induced transient response as the switching of transistors Q1–Q6 is altered during the V_{bus} change.

A preferred solution to this anomaly is illustrated in FIG. 8 which is similar to the circuit diagram of FIG. 5 or 6 except for the additional inclusion of a feed-forward connection. The feed forward connection preferably includes, for example, a ramp generator receiving V_{bus} as an input and periodically reset to produce a ramp function having a fixed frequency controlled by an independent or otherwise available clock. Therefore the peak voltage of the ramp, V_{pp} , is proportional to V_{bus} and V_{bus} controls the ramp slope. When this ramp voltage is provided to the negative input of a voltage comparator having a constant voltage V_c supplied to a positive input thereto, the output of the voltage comparator will change after a period D for each ramp such that $D \times V_{bus} = \text{Constant}$. Thus, D is inversely proportional to V_{bus} . This period is applied to adjust the switching timing of Q1–Q6 (or Qn) in the second stage circuits to alter their

switching periods to compensate for the transient change in V_{bus} concurrently with the occurrence of that change. Therefore V_o is made immune to V_{bus} variation. The efficacy of this solution is illustrated in FIG. 9. Accordingly, the arrangement of FIG. 8 is considered to be preferred for the first embodiment of the invention and it is readily seen, when it is considered that the current load in all of the sleep states, while different from each other are all in a region of FIG. 3B which is substantially optimal and below the minimum practical value of V_{bus} , that the preferred arrangement provides a substantially optimal positioning of V_{bus} for all loads except for the extremely brief periods of low current load in the C0 state and the similarly short periods of high current load outside the C0 state.

In seeking to address the variation in V_o which may occur during such short transient periods which are the only periods in which the preferred basic embodiment of the invention does not optimally position V_{bus} , it is ideally desired to make the positioning of V_{bus} adaptively adjustable to the actual instantaneous current load. These changes are graphically depicted in FIGS. 10A and 10B, the latter of which is essentially a detail of FIG. 1 and particularly indicating periods of less than maximum current load during C0 state periods when the positioning of V_{bus} at one of two nominal discrete voltages is not ideal. To be ideal, the V_{bus} voltage would be required to assume some additional voltage levels, as shown in FIG. 10B. Further, differences in the load may induce changes in V_o as shown in FIG. 10A. For example, as shown in FIG. 10A, if there is a transient increase in current load while V_{bus} is low, V_o will slightly decrease or droop. Conversely, during periods of reduced current load while V_{bus} is high, V_o will slightly increase. The voltage droop may even be specified by CPU manufacturers to regulate power dissipation at high loads. It should also be recognized, as shown in FIG. 10B, that intermediate levels of current load may be presented between maximum load presented during the C0 state during which droop will (or must) occur to some degree and also between the various respective sleep states C1–Cn during which droop is slight or should be avoided.

Accordingly, as a perfecting feature of the invention, it is proposed to provide a voltage tilt in V_{bus} to adjust otherwise discrete voltage levels to even more precisely optimize V_{bus} . It should be noted that the tilt and droop functions illustrated in FIG. 10A are substantially linear functions of voltage variation with current and can thus be characterized as resistances, R_{tilt} and R_{droop} . Further, as a matter of terminology and to emphasize the respective functions of the basic invention described above with reference to FIGS. 1–9 which provides selected, discrete levels of V_{bus} voltage depending on load operational state and referred to as Adaptive voltage positioning@ (AVP), the perfecting feature to be described below with reference to FIGS. 10–12 is referred to as “adaptive bus voltage positioning” (ABVP) in which adjustments are made in both the first and second regulator stages to provide alteration of V_o with transient load current changes as may be required as well as to more fully optimize efficiency of the voltage regulator by providing a V_{bus} voltage even more accurately matched to the actual load.

This is preferably accomplished in accordance with the circuit shown in FIG. 11. In the first stage of this circuit, a reference voltage or other signal (e.g. signal from current sensor i_L) from the ACPI is coupled to a positive mixing node of a voltage comparator 130 to adaptively alter V_{bus} based on operating state while V_{bus} is fed back to the negative mixing node to control switching of Q11 and Q22

to obtain the desired V_{bus} voltage, generally as described above. However, in this perfecting feature of the invention, the feedback of the V_{bus} voltage includes a resistor, R_{tilt} . Since, as generally shown in FIG. 2, the optimum V_{bus} value shifts substantially linearly with load current, the value of R_{tilt} can be determined directly from the maximum current load and the maximum and minimum practical V_{bus} values. In the second stage of the circuit both the output voltage V_o and current I_o are sensed and applied to positive mixing nodes of a voltage comparator 160. The sensed voltage is attenuated by a resistor having a value, R_{droop} , proportional to the slope of the permitted or required voltage droop with change of output current I_o and mixed with a signal representing the output current. The resulting (mixed) voltage signal is compared with a reference voltage V_{ID} (an internal digital voltage specification provided by the processor). A feedback arrangement including this V_o and I_o information may be required by the particular CPU or other load powered by V_o and is generally provided in the voltage regulator. The output of voltage comparator 160 is used to adjust the reference value V_c discussed above in connection with the feed forward solution to the V_o anomaly when V_{bus} is changed in accordance with the invention as discussed above.

In accordance with this form of the first embodiment of the invention, the current measurement used for the second stage feedback is also fed back to the first stage and applied to a mixing node of voltage comparator 130 to adjust the switching of Q11 and Q12 to adjust V_{bus} . In this regard, some switching, as will be evident to those skilled in the art (e.g. from a negative mixing node to a positive mixing node), may be required to avoid producing voltage droop at low current loads when V_{bus} is low. Thus the load current information, i_L , usually already available in the second (or single) stage of a voltage regulator, is injected into the feedback loop of the first stage to adaptively adjust the present V_{bus} level in accordance with the first embodiment of the invention or provide the entire V_{bus} positioning function in accordance with a second embodiment of the invention while the feed forward arrangement is still advantageously used by adaptive bus voltage positioning (ABVP).

As alluded to above, it is not only possible but preferred for simplicity in accordance with a second embodiment of the invention to provide the entire V_{bus} positioning function based on the current feedback information i_L and omitting the operating state information 140. This second embodiment has the additional advantage that switching transients due to the lower control bandwidth of the first stage may be less severe and the number of information paths in the feedback arrangement to the first stage is reduced and feedback control design simplified but may be limited in regard to precision of synchronization with the operational state since changes in the actual load cannot be measured in advance although any limitation in this regard is likely to be slight. In this case, i_L is simply fed back to the negative mixing node for the negative input of voltage comparator 130 to provide continuous adjustment over the entire practical range for positioning of V_{bus} .

The design principles of the ABVP-AVP system of FIG. 11, illustrating both the first embodiment of the invention with the perfecting feature described above or the second embodiment of the invention in which the V_{bus} positioning function is based on the actual current load are illustrated in FIG. 12 which graphically illustrates simulated performance of a voltage regulator in accordance with the second embodiment of the invention for a negative-going change in load current at time t_0 . (Similar data would be expected for

the first embodiment with the perfecting feature described above.) A similar but opposite response occurs for a positive-going change in load current. During the period from t_0 to t_1 , corresponding to the finite rise or fall time of the load current information, i_L , there is little change in V_{bus} and V_o responds to the I_o change (with voltage regulation performance enhanced by feedback in the high-frequency response second stage of current load information, i_L , determined by the second stage control loop as i_L changes). Therefore, it is clear that the second stage can be designed independently of the first stage and the two-stage arrangement providing optimal V_{bus} in the first stage can be used in any voltage regulator design. After t_1 , when i_L becomes effective to adjust V_{bus} , V_o and i_L are immune to V_{bus} variation and the first stage design follows voltage-mode control design as described above which provides an optimum discrete V_{bus} voltage level for optimum voltage regulator efficiency responsive to the operational state of the load which can be further adjusted, preferably over a continuous range of voltages which may exceed the range of V_{bus} voltages provided by the basic invention, based on actual measured I_o . Thus, in accordance with the first embodiment of the invention, large changes in load can be accommodated in a manner closely synchronized with the actual load by switching the coarse value of V_{bus} based on prior knowledge of the operating state while smaller changes in load (or the entire change in load in accordance with the second embodiment of the invention) may be accommodated rapidly by feedback of actual current load information and with minimization of transients due to voltage regulator switching or analog transient response and, in both embodiments, increased efficiency by closer matching of V_{bus} to the actual current loads particularly for very large and very small (e.g. sleep state) loads and variations in load during working mode or a sleep state.

As noted above, V_{bus} cannot respond to high frequency load transients (e.g. in the MHz range. FIG. 13 illustrates that, using ABVP, the first stage is able to provide varying levels of V_{bus} which track all of the CPU operating states C0–Cn including the C0–C1 transients in C0 states and the efficiency of the voltage regulator in accordance with the invention is optimal, even for transients within the C0 state as long as the recurrence frequency is below the MHz range (e.g. C0 transient groups A and B). The ability of the first stage to provide a range of voltages using ABVP in accordance with the perfecting feature in the first embodiment of the invention or using the second embodiment of the invention also provides optimal efficiency at high recurrence frequency of transients and near-optimal efficiency at intermediate frequency as will now be discussed in connection with FIGS. 14A–14D.

FIG. 14A shows the AVP and ABVP response to varying current loads at low recurrence frequency below the first stage control bandwidth. It can be readily seen that V_{bus} closely tracks variations in I_o and regulation of V_o is good (e.g. within 0.09 volts, as shown). Both stages see the instantaneous I_o and optimal V_{bus} is determined as discussed above. FIG. 14B illustrates response of the voltage regulator in accordance with the invention with a load transient recurrence frequency above the second stage control bandwidth. In this case, both the first and second stages only see the average value of I_o and the optimal value of V_{bus} is determined accordingly based on the average load current; variations in which are shorter than the current ripple in the inductors of both the first and second stages and thus an optimal V_{bus} voltage, in fact, corresponds to the average load current and transients are handled by the output filter capaci-

tor Co, as illustrated in FIG. 14C. However, as shown in FIG. 14D, if the recurrence frequency of the load transients is between the control bandwidths of the first and second stages, the second stage sees the instantaneous I_o transients while the first stage sees only the average I_o . Thus, there will be increased current ripple in the inductors of both the first and second regulator stages. However, as shown in FIG. 15, the loss of efficiency is small while good voltage regulation is maintained. Specifically, the variation in V_o remains in the same range as in FIG. 14A (including droop, as may be required) while V_{bus} will exhibit a small ripple around an average value determined by the duty cycle of the current load transients. Since the loss of efficiency corresponds to the variation in V_{bus} from its optimal value, the variance of efficiency from its optimal level will generally be reduced by the size of the ripple in V_{bus} as it follows the instantaneous average of I_o and thus is much more closely matched to the optimum V_{bus} value than has previously been possible, regardless of the design point chosen for a fixed V_{bus} value.

In the present invention, the first and second regulator stages can comprise many different kinds of regulators. For example, the first stage can comprise a multi-phase buck regulator, which is capable of providing a variable V_{bus} voltage. Other kinds of regulators that can provide the variable V_{bus} voltage and can be used in the first stage include full bridge, half bridge, forward or push-pull regulators.

Also, the second stage can comprise a full bridge, half bridge, forward or push-pull regulator. Any of these kinds of regulators will provide the benefit of increase power conversion efficiency when employed as the second stage regulator and receiving the variable V_{bus} voltage supply. Hence, the present invention and appended claims should be understood to include many different kinds of voltage regulators, connected in series.

An important consequence of the present 2-stage regulator is that the second stage operates at a reduced voltage, and can therefore employ switches with a reduced voltage rating. For example, in a prior art single stage regulator, 30 volt switches may be required, which tend to have high internal resistance values (Rds-on values). By comparison, in the present invention, since the second stage regulator may operate at a nominal voltage in the range of 3–6 volts, lower voltage rating switches (e.g. rated at 12–15 volts) can be used. Low voltage rating switches tend to have much lower internal resistance values, and consequently lower conduction losses.

A further consequence of the reduced operating voltage of the second stage is that the operating frequency can be greatly increased. For example, reducing the operating voltage from 12 volts to about 5 volts can allow an increase in operating frequency from about 350 Khz to about 2 Mhz. This enormous increase in frequency provides other benefits such as allowing for smaller output capacitors and inductors to reduce current ripple, and offering faster transient response.

In conclusion, compared with a single stage regulator, the present two-stage regulator can achieve higher efficiency at higher switching frequencies. Additionally, the size and cost of filtering components (capacitors and inductors) can be reduced. Hence, the advantages of the present two-stage regulators are particularly great when the second stage is made to operate at frequencies of about 1 or 2 Mhz, and the second stage switch devices have voltage ratings in the range of about 5–15 volts.

In another aspect of the present invention, the operating frequency of the second stage is adjusted as output current

changes. Adjustment of the operating frequency allows for further efficiency improvements (about 2–3% primarily in the low-load regime), and can provide a output current ripple of constant magnitude (over the entire range of output current).

FIGS. 16A and 16B show aligned plots of regulator efficiency and normalized peak-to-peak output current ripple. As the Vbus voltage increases from 3 volts to 6 volts, the output current ripple increases monotonically. This is because the output current ripple from a buck regulator varies according to the following equation:

$$\text{Ripple} = V_{\text{out}} / Lf(1-D)$$

where Ripple is the peak-to-peak current ripple, Vout is the output voltage, L is the output inductance, f is the switching frequency (for each phase), and D is the duty cycle. Accordingly, the output current ripple varies as shown in FIG. 16B.

The variation in output current ripple presents a problem in regulator. Specifically, the ripple must be lower than a certain value at all times. However, designing the circuit to accommodate the largest possible ripple requires large filtering components that are unnecessarily large for operating regimes that produce small current ripple. In order to circumvent this problem, and provide other benefits (e.g. increased efficiency) in the present invention, the switching frequency of the second stage is adjusted as the Vbus voltage is adjusted. Specifically, the switching frequency can be adjusted such that either 1) the output current ripple is held constant or, 2) the operating efficiency is maximized. These two desired endpoints might or might not coincide in a particular control scheme for the switching frequency.

Since the switching frequency is inversely proportional to the output voltage, constant ripple magnitude can be achieved by adjusting the switching frequency according to the same curve illustrated in FIG. 16B.

FIG. 17 for example, illustrates such an embodiment in which the switching frequency varies from about 700 Khz to about 1 Mhz. With the switching frequency of the regulator stage (comprising single or multiple parallel buck regulators) controlled according to the plot of FIG. 17, the output current ripple will be approximately constant as Vbus voltage varies and output current varies. With the output current ripple held constant to a value lower than the maximum ripple in the constant-frequency embodiment, the output filtering components can be reduced in size. When the output current ripple is held constant, there is no concern that the filtering capabilities of the capacitive and inductive output components will be exceeded in the high current regime. It is noted that, in the operating regime where Vbus voltage is held constant (e.g. below about 10 A, as illustrated in FIG. 3B), the switching frequency is also held constant. The switching frequency is adjusted only to counteract the effect of the variable Vbus voltage on output current ripple.

FIG. 18 shows plots of conversion efficiency versus output current for an embodiment having fixed switching frequency (and variable output current ripple), and for an embodiment having variable switching frequency (and constant output current ripple). As can be observed in FIG. 18, the variable switching frequency increases the efficiency by about 2–3%, particularly in the low output current regime. The conversion efficiencies of the embodiments are approximately equal in the high output current regime (above about 25 A).

In conclusion, the variable switching frequency of the second stage regulator provides two substantial benefits in combination: increased efficiency and constant output cur-

rent ripple. It is noted that the conversion efficiency might be increased by slightly altering the relationship between the switching frequency and output current (i.e. by altering the shape of the curve in FIG. 17).

In view of the foregoing, it is readily seen that the invention provides a voltage regulator which is capable of high-quality regulation over an extremely wide range of current loads while maintaining optimal efficiency under all load and transient conditions except for transient recurrence frequencies between the control bandwidths of the first and final stages which generally will be encountered only rarely and/or for only brief periods of time at extremely low duty cycles. The voltage regulator in accordance with the invention is particularly well-suited to and highly compatible with sophisticated power saving arrangements, particularly where very large and very small loads are presented for the predominant amount of time during use where prior voltage regulators have presented conflicting design criteria and exhibited substantial and previously unavoidable inefficiency. Embodiments of the invention suitable for use with CPUs in laptop computers and the like are of particularly simple configuration and can be fabricated at small size and light weight. Power dissipation requirements are thus reduced and usable battery life can be significantly extended.

While the invention has been described in terms of two preferred embodiments and a perfecting feature for the first embodiment, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

We claim:

1. A two-stage power converter, comprising:

- a) a first regulator stage providing an adjustable bus voltage Vbus;
- b) a second regulator stage receiving the bus voltage Vbus and providing an output current;
- c) a current sensor for sensing an output current of the second regulator stage; and
- d) a control circuit responsive to an output of the current sensor, wherein the control circuit controls steady state operation of the first regulator stage such that the bus voltage Vbus increases with increasing output current.

2. The two-stage power converter of claim 1 wherein the second stage comprises a plurality of buck regulator phases connected in parallel.

3. The two-stage power converter of claim 2, wherein the plurality of buck regulator phases are activated according to output current, wherein the number of active phases increases with increasing output current.

4. The two-stage power converter of claim 2 wherein one of the plurality of buck regulator phases includes switches with a current rating less than 1/5 the current rating of switches in the other parallel-connected buck regulator phases.

5. The two-stage power converter of claim 2 wherein one of the plurality of buck regulator phases includes switches with a current rating less than 1/10 the current rating of switches in the other parallel-connected buck regulator phases.

6. The two-stage power converter of claim 1 wherein the control circuit varies a duty cycle or operating frequency of the first regulator stage to adjust the bus voltage Vbus.

7. The two-stage power converter of claim 1 wherein a switching frequency of the second regulator stage is responsive to Vbus voltage such that a switching frequency increases with increasing Vbus voltage.

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8. The two-stage power converter of claim 7 wherein the switching frequency increases at a rate selected such that an output current ripple varies less than 10% when output current varies over a normal operating range.

9. The two-stage power converter of claim 1, wherein the first regulator stage and second regulator stage comprise a regulator selected from the group consisting of buck, multiple phase buck, full bridge, half bridge, forward and push-pull regulators.

10. A two-stage power converter, comprising:

- a) a first regulator stage providing an adjustable bus voltage V_{bus} ;
- b) a second regulator stage receiving the bus voltage V_{bus} and providing an output current;
- c) a current sensor for sensing an output current of the second regulator stage;
- d) a control circuit responsive to an output of the current sensor, wherein the control circuit controls steady state operation of the first regulator stage such that the bus voltage V_{bus} increases with increasing output current, and

wherein a switching frequency of the second regulator stage increases with increasing V_{bus} voltage.

11. The two-stage power converter of claim 10 wherein the second stage comprises a plurality of buck regulator phases connected in parallel.

12. The two-stage power converter of claim 11, wherein the plurality of buck regulator phases are activated according to output current, wherein the number of active phases increases with increasing output current.

13. The two-stage power converter of claim 11 wherein one of the plurality of buck regulator phases includes switches with a current rating less than $\frac{1}{5}$ the current rating of switches in the other parallel-connected buck regulator phases.

14. The two-stage power converter of claim 11 wherein one of the plurality of buck regulator phases includes switches with a current rating less than $\frac{1}{10}$ the current rating of switches in the other parallel-connected buck regulator phases.

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15. The two-stage power converter of claim 10 wherein the control circuit varies a duty cycle or operating frequency of the first regulator stage to adjust the bus voltage V_{bus} .

16. The two-stage power converter of claim 10 wherein the switching frequency varies at a rate selected such that an output current ripple varies less than 10% when output current varies over a normal operating range.

17. The two-stage power converter of claim 10, wherein the first regulator stage and second regulator stage comprise a regulator selected from the group consisting of buck, multiple phase buck, full bridge, half bridge, forward and push-pull regulators.

18. A two-stage power converter, comprising:

- a) a first regulator stage providing an adjustable bus voltage V_{bus} ;
- b) a second regulator stage receiving the bus voltage V_{bus} and providing an output current;
- c) a current sensor for sensing an output current of the second regulator stage; and
- d) a control circuit responsive to an output of the current sensor, wherein the control circuit controls steady state operation of the first regulator stage such that the bus voltage V_{bus} increases with increasing output current; wherein the second stage comprises a plurality of buck regulator phases connected in parallel, and wherein the plurality of buck regulator phases are activated according to output current, wherein the number of active phases increases with increasing output current.

19. The two-stage power converter of claim 18 wherein one of the plurality of buck regulator phases includes switches with a current rating less than $\frac{1}{5}$ the current rating of switches in the other parallel-connected buck regulator phases.

20. The two-stage power converter of claim 18 wherein a switching frequency of the second regulator stage is responsive to V_{bus} voltage such that a switching frequency increases with increasing V_{bus} voltage.

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